Designing the EMI-Performance of Mixed Signal Circuits by Nonperiodic Clocking

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Abstract— *Spread spectrum technique is an efficient method to shape the EMI spectrum of mixed signal circuits. However due to problems in spectrum calculation the applications found are limited. A new method is chaotic clock generation. This paper proposes classical methods and spread spectrum clock generation for EMI reduction and their impact on the EMI spectrum of mixed signal circuits. Realisations of spread spectrum clock generation are proposed. The impact of chaotic clock generation on EMI is shown in a charge pump realisation.*

I. Introduction

Mixed signal circuits work on the base of switching voltages and/or currents. This causes current AC components at the supply line V_{DD} which results in electromagnetic interference (EMI). An important criterion to assess EMI is the power density spectrum (PDS) of the current I_{DD} at the supply line. In order to fulfil EMC conventions[1] limiting the power density maxima is of basic interest during the design. Classical solutions to reduce EMI like filtering the supply voltages and pulse shaping distribute the energy between the harmonics. Newer methods modulate the clock frequency and spread the energy around the multiples of the clock frequency. In this paper classical methods and their impact on the PDS are treated overview like in section III. The main part will be concentrated on clock frequency modulation. In section V we propose schematics for the most important blocks of a chaotic clock generator using iterative return maps. The EMI reduction of a charge pump by nonperiodic clocking is investigated in section VI.

[1] EMC: Electromagnetic Compatiblity

II. EMI in Mixed Signal Circuits and EMC Conventions

A. EMI in Mixed Signal Circuits

The reason for EMI in mixed signal circuits are the switching processes in the circuit at each clock event. Due to this switching the supply line current takes different functions. Two examples are shown in Fig. 1. If the current signal is periodic then it has a discrete

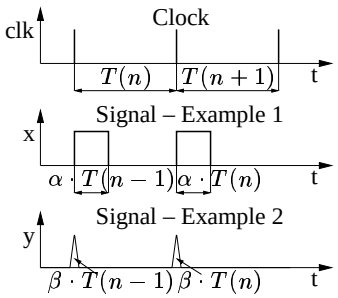

Fig. 1. Clock signal and corresponding current signals – examples

PDS and the power is concentrated in the harmonics.

B. EMC Conventions

As EMI can cause malfunction in other systems EMC conventions (e.g. [1]) were made to ensure proper function of devices without disturbing other devices or being disturbed in the EMI polluted environment near to other systems.

Therefore two steps are neccesary: limiting the system-caused EMI and make the system resistable against received EMI. This paper is focused on limiting the EMI spectrum. To reach this the maximum power density is limited in form of a function of frequency.

Fig. 2 depicts the predicted piecewise linear upper limit curve of the PDS consisting of three segments (constant amplitude, 20dB/Dec. decreasing, 40dB/Dec. decreasing) according to IEC 61967-

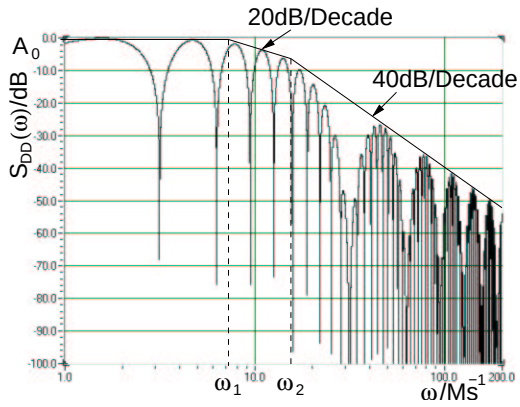

Fig. 2. Limit curve of the PDS according to IEC 61967-4

4. The segments are parametrised by translating them parallel to the amplitude axis in the diagram. The specification of the limit is then done by three parameters according to the segments of the limit curve (e.g. H11m with H parametrising A_0 and 11 and m parametrising the parallel translation of the 20dB/Dec. and 40dB/Dec. segments respectively).

The task of the designer is to get the complete PDS of the supply line current below the predicted limit curve. Therefore several methods are possible.

III. Classical Methods to reduce EMI

A. EMI Filter

The oldest method to reduce the power density maxima is using an EMI filter. This is a lowpass filter switched between the power supply and the circuit. The filter cuts the harmonics and moves energy to the mean value. Moving energy to the mean value is the savest way to prevent disturbation of other systems.

Due to the high efficiency in reducing circuit-generated EMI passed thrue the supply as well as EMI on the supply line (from another system) passed thrue the circuit this method is used in most devices. However it is very expensive because the supply current passes the filter and therefore power devices are required.

Due to the limited integrability of inductors and the small value of integrated capacitors EMI filters are not realisable on chip and hence also in integrated low power devices EMI filters lead to significant additional coast due to required chip-external components.

B. Pulse shaping

Pulse shaping affects the current functions shown in Fig. 1. Therefore the switching process is controlled continuously. An example of pulse shaping is converting the rectangular current $I_{DD}(t)$ into a sin-wave like one by pulse shaping to reduce the energy in the higher harmonics.

The seemingly advantage of this method is the low-coast realisation in the controlling part of the circuit without power components. But the “slowly switching” increases the power loss in many systems (e.g. in the switching transistor of DC-DC converters) and hence significantly reduces their efficiency.

This method is only able to distribute the energy between the harmonics, which is another disadvantage. If the higher harmonics are reduced by pulse shaping the power in lower harmonics is increased. Pulse shaping cannot cut them.

This method is mostly used in IC realisations of switched power supplies (e.g. integrated charge pumps) where an EMI filter is not implementable.

IV. Nonperiodic Clock

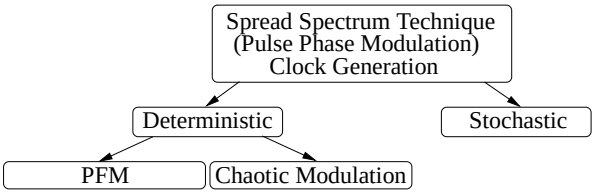

Fig. 3. Spread spectrum clock generation techniques

In nonperiodic clocked systems the energy is spread around the medium clock frequency and its multiples. Hence the maximum power densities are reduced. Nonperiodic clock signals can be generated using deterministic and stochastic generation schemes (Fig. 3). Deterministic schemes use a return map g to generate a sequence of values $x(n)$ which is converted into subsequent time intervals $T(n)$ with a value-to-time converter (VTC)

$$x(n+1) = g(x(n)) \tag{1}$$

$$T(n) = f(x(n)) \; . \tag{2}$$

A. Periodic Frequency Modulation

In case of periodic frequency modulation (PFM) g and f can be merged. Examples of PFM are the linear interval time sweep

$$T(n+1) = \begin{cases} T(n) + \theta & z(n) = 1 \\ T(n) - \theta & z(n) = 0 \end{cases} \tag{3}$$

with a boolean variable

$$z(n+1) = \begin{cases} z(n) & T_{min} < T(n-1) < T_{max} \\ \overline{z(n)} & else \end{cases} \; . \tag{4}$$

θ is the time increment.

Another example is the linear frequency sweep. Fig. 4 depicts a system realisation. A waveform gen-

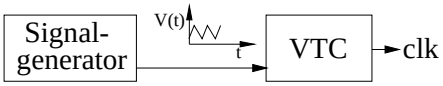

Fig. 4. System for periodic frequency modulation

erator produces a triangular like signal controlling a VTC.

The controlling signal $V(t)$ is directly proportional to the modulated clock frequency f. Fig. 5 shows the resulting frequency dependence $f(t)$. T_m and Δf are the modulation period and the clock frequency swing respectively.

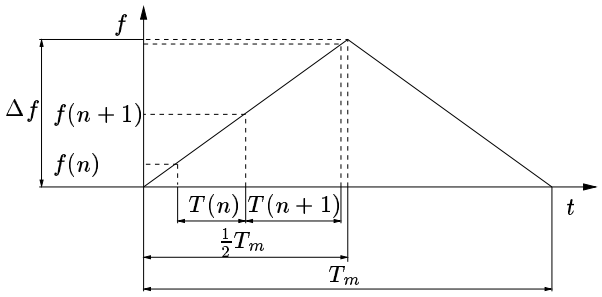

Fig. 5. Periodic frequency modulation

The generated time sequence can be described as follows: At the end of step n the frequency $f(n)$ for the next period $T(n)$ is set. At the end of $T(n)$ the next frequency $f(n+1) =$

$$\frac{1}{T(n+1)} = \begin{cases} \frac{1}{T(n)} + \mu \cdot T(n) & z(n) = 1 \\ \frac{1}{T(n)} - \mu \cdot T(n) & z(n) = 0 \end{cases} \quad (5)$$

is set with

$$\mu = 2 \cdot \frac{\Delta f}{T_m} \quad (6)$$

is the frequency slope (see Fig. 5).

Design variables are the modulation index

$$m = \frac{T_{max} - T_{min}}{\overline{T}} = \frac{f_{max} - f_{min}}{\overline{f}} \quad (7)$$

and the modulation period T_m.

Figs 6, 7 and 8 show the calculated EMI spectrum around the medium clock frequency for the linear frequency sweep using $f_m \approx \frac{1}{1000} f$ for different modulation indices. This shape reappears at the multiples of the medium clock frequency. Due to the linear frequency sweep the EMI spectrum has a nearly rectangular shape. This shape achieves a maximum

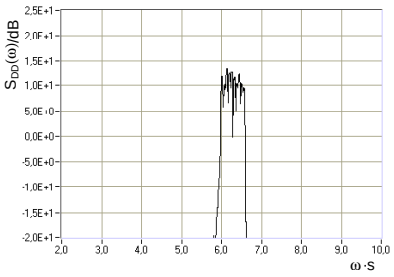

Fig. 6. EMI spectrum of a PFM clock system, $m \approx 0.1$

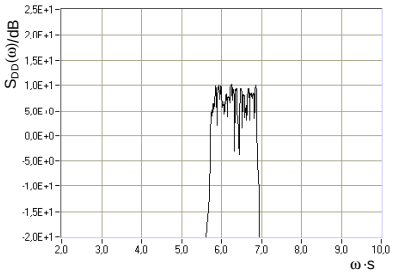

Fig. 7. EMI spectrum of a PFM clock system, $m \approx 0.18$

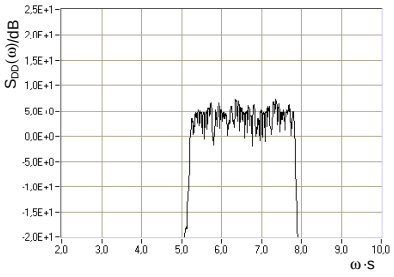

Fig. 8. EMI spectrum of a PFM clock system, $m \approx 0.67$

EMI suppression at a predicted m. The maximum power densities decrease with rising m. The widths of the spectral maxima are $m \cdot \overline{f}$ for the medium clock frequency and $o \cdot m \cdot \overline{f}$ for the multiples o of the medium clock frequency. Hence the EMI suppression increases with rising o until the bands overlap. After reaching overlapping the suppression remains constant.

The rectangular PDS shape is only achieved with with a modulation frequency $f_m \ll \overline{f}$. With rising f_m the PDS shape changes from a rectangular into a beaked one resulting in worse EMI suppression.

In [2] the linear frequency sweep method is investigated more in detail. Typical applications are found in motherboard clock generation for PC with $m = 0.5/2.5\%$ [3].

B. Chaotic Modulation

In the chaotic case g in Eq. (1) is a chaotic return map. Fig. 9 shows a possible system realisation.

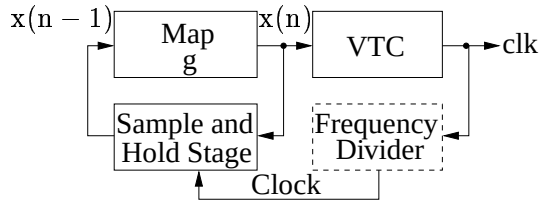

Fig. 9. Nonperiodic clock frequency modulation using an iterative return map

During one clock phase the sample and hold stage (S&H) connects the signal $x(n-1)$ to the input of the nonlinear map g. The corresponding output signal $x(n) = g(x(n-1))$ is sampled simultaneously. In the next clock phase $x(n)$ is connected to the input of the map g and $x(n+1)$ is sampled. The sequence $x(n)$ controls a VTC generating the clk signal. A frequency divider between clk and Clock can be used to get a constant duty cycle or a subsequence of n clocks at constant $T(n)$.

Here the design variables are the map g, the modulation index m and the divisor of the frequency divider. The modulation index is determined as follows: Assuming input and output interval of $g \in [0,1]$ and $f(x)$ in Eq. 2 to be monotonous. Then m is obtained by

$$m = \frac{|f(1) - f(0)|}{\overline{T}} \tag{8}$$

where

$$\overline{T} = \int_0^1 f(x)dx \tag{9}$$

is the medium clock period.

Figs 10 to 13 depict the PDS arround the medium clock frequency of a system using a bernoulli map and tent map clock generator respectively with different m. Eq. (2) was set to $f(x) = T_0 + \alpha \cdot x$. The shapes depicted in Figs. 10 to 13 repeat for multiples o of the medium clock frequency $\overline{f}$ in the same way like PFM. The increasing EMI suppression for multiples o of $\overline{f}$ behaves similar to PFM.

Note that the EMI suppression is not as good as the achievable suppression by using PFM. To get the suppression of PFM a higher modulation index than the PFM one is required depending on the Lyapunov exponent λ of the chaotic system. Strong chaotic systems (large positive λ) exhibit more narrow PDS shapes than weak chaotic (small positive λ) ones and hence require a larger m for good EMI reduction.

The difference between the spectra of strong chaotic and weak chaotic systems is analogous to PFM with $f_m \approx \overline{f}$ and $f_m \ll \overline{f}$ respectively which results in the presumption that clock modulation with

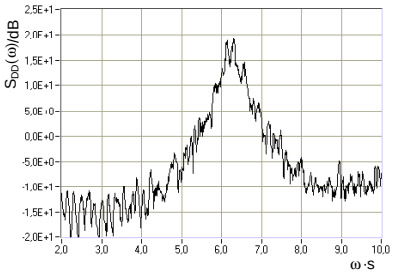

Fig. 10. EMI spectrum of a bernoulli map clock system, $m \approx 0.18$

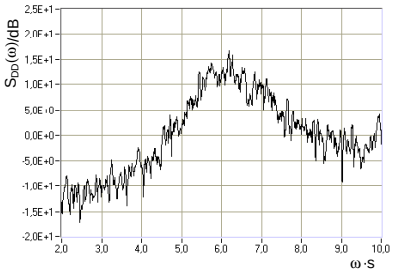

Fig. 11. EMI spectrum of a bernoulli map clock system, $m \approx 0.67$

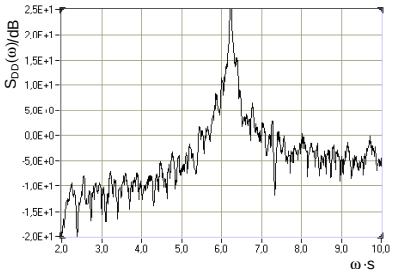

Fig. 12. EMI spectrum of a tent map clock system, $m \approx 0.18$

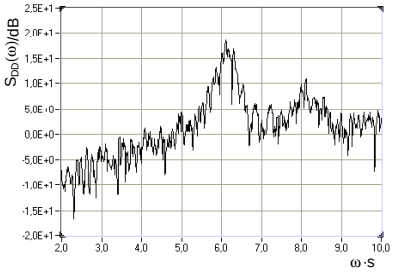

Fig. 13. EMI spectrum of a tent map clock system, $m \approx 0.67$

slow varying clock frequency in general achieves better EMI suppression than a fast varying clock frequency modulation.

Hence a weighty step in chaotic signal generator design is choosing an appropriate map.

B.1 Value-to-Time Conversion

A general system for value-to-time conversion is depicted in Fig. 14. It consists of an integrator with integration constant c, two comparators and a RS flip flop controlling S_1. After reaching the thresholds V_{r+} and V_{r-} the system switches between the states integrate up and integrate down respectively. Duty cycle and clock frequency are determined by

$$T_{H/L} = \frac{V_{r+} - V_{r-}}{c \cdot V_{i+/-}} \tag{10}$$

where adjusting V_{r+} and V_{r-} corresponds to time modulation and adjusting V_{i+} and V_{i-} corresponds to frequency modulation.

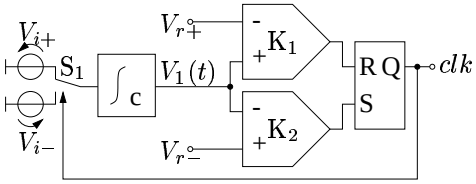

Fig. 14. Value-to-time conversion – system 1

Another system converting a value into time uses a constant frequency clock signal instead of K_2 (Fig. 15). Note that the system itself includes a nonlinear map and hence under specific conditions can exhibit chaotic behaviour without any external exitation. This system exactly corresponds to a current mode dc-dc converter [4].

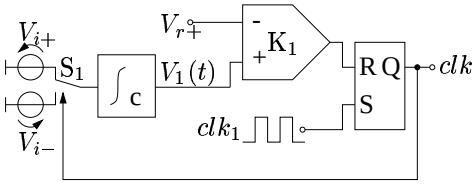

Fig. 15. Value-to-time conversion – system 2

V. Realisation of Chaotic Clock Generation

In this section we propose realisations of the most important blocks of a chaotic clock generator, the iterative return map and the VTC. For sample and hold circuits there exists an amount of literature. They are not treated in this paper.

A. Iterative Return Map

Here we concentrate on piecewise linear maps which are easy to realise. For that the following functions are required: reference, scaling, comparator and switch. Current technique offers the possibility to realise all these blocks with a few components. We present two piecewise linear maps in current technique. In principle every piecewise linear map can be realised with the blocks proposed here.

A.1 Tent map

Fig. 16 depicts the schematic of the tent map realisation. It consists of of the current mirrors Mi_1 and Mi_2 and a reference I_0. The numbers at the transistors indicate their normalised W/L ratio.

If the input current is lower than $\frac{1}{2}\mathrm{I}_0$ Mi_2 is deactivated due to the negative input current I_{2a}. Then I_{2b} is zero and

$$I_{out} = 2 \cdot I_{in} \tag{11}$$

corresponds to the first segment of the map. By exceeding $\frac{1}{2}\mathrm{I}_0$ Mi_2 becomes active (comparator behaviour) resulting in

$$I_{out} = 2 \cdot I_{in} - I_{2b} = 2 \cdot (I_0 - I_{in}) \tag{12}$$

and the second segment is mapped.

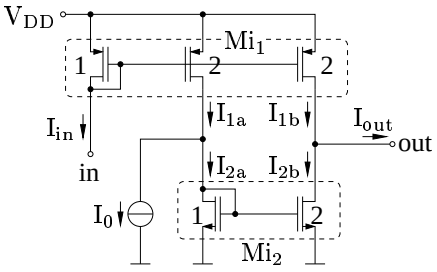

Fig. 16. Tent map in current technique

A.2 Bernoulli map

The bernoulli map is realised by two current mirrors Mi_1 and Mi_2, a reference source I_0 and a switch S_1 (Fig. 17). Here the comparator consists of M_1, M_2 and S_1. S_1 switches on if I_{in} exceeds $\frac{1}{2}\mathrm{I}_0$ ($\mathrm{I}_{1a} > \mathrm{I}_{2a}$). Then the second segment

$$I_{out} = 2 \cdot (I_{in} - I_0) \tag{13}$$

is mapped. If I_{in} is below $\frac{1}{2}\mathrm{I}_0$ S_1 is off and hence $\mathrm{I}_{2b} = 0$. Then the first segment is mapped the same way like in the tent map circuit.

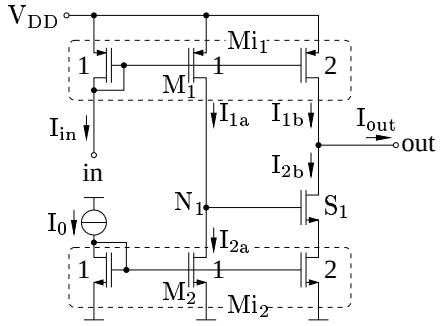

Fig. 17. Bernoulli map in current technique

B. Value-to-Time Converter

An easy to realise VTC is a source coupled oscillator [5]. The corresponding schematic is depicted in

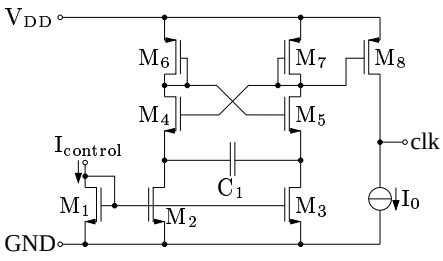

Fig. 18. Source coupled oscillator

Fig. 18. M_1, M_2 and M_3 are a current mirror sourcing the controlling current $I_{control}$ to charge C_1. M_6 and M_7 are the load for M_4 and M_5 respectively. The task of M_8 and I_0 is to provide a rail to rail clk.

Assuming M_4 to be active the voltages at drain and source of M_4 are fixed and M_5 is off. Then M_3 charges C_1 and the voltage at the source of M_5 falls until M_5 reaches its threshold value. That followed M_5 turns on and switches M_4 off and the complementary process begins.

The frequency is adjusted by $I_{control}$ determining the charging time. This corresponds to adjusting V_{i+} and V_{i-} in Fig. 14. However note that the thresholds V_{r+} and V_{r-} also depend on $I_{control}$ since the voltages at the drains of M_4 and M_5 are current dependent. This leads to a nonlinear dependence between f and $I_{control}$.

VI. A chaotic clocked Charge Pump

A. Charge Pump and Clock Generator

For investigation of the impact of chaotic clock generation on the EMI spectrum we implemented a tent map clock generator into a single stage charge pump (Fig. 19) and calculated the corresponding PDS S_{DD} of I_{DD}.

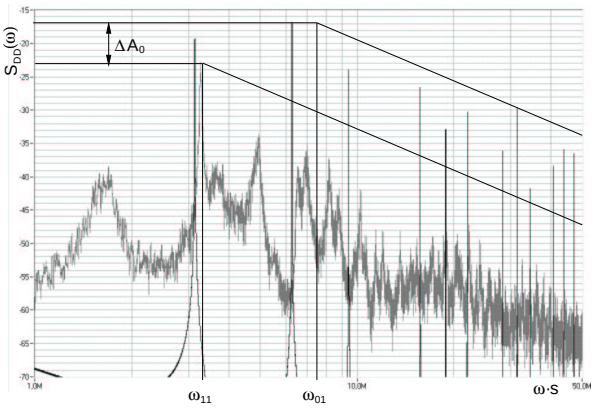

Fig. 20. Comparison between the spectra of a charge pump using unmodulated and chaotic generated clock signal

The structure of the charge pump is typical for high voltage asics. The input voltages are the stabilised core voltage $V_{DD} = 5V$ and the unstabilised high voltage V_{PP} (e.g. $12 \ldots 60V$). During the first clock phase the driver switches V_{Dr} to zero and C_1 is loaded via D_1. In the second clock phase the driver switches V_{Dr} to V_{PP} and the external storage capacitor C_{Load} is charged up to approximately $V_{C_1} + V_{PP}$ via D_2. This results in an output voltage V_{Pump} which is situated at a constant value above the unstabilised high voltage. Depending on the specified output voltage V_{Pump} the charge pump can have more stages. We implemented a current limitation into the charge pump resulting in a rectangular pulse shape of $I_{DD}(t)$.

The implemented clock generator is based on the realisation in Fig. 9 using the tent map (Fig. 16) and the source coupled oscillator (Fig. 18). The period time varies between $1.6\mu s$ and $3.2\mu s$.

B. Results

Fig. 20 depicts S_{DD} using periodic and chaotic clock signal. To rate the EMI improvement the piecewise linear envelopes of the spectra according to the EMC conventions are shown. The improvement is about 6dB in the first region ($\omega < \omega_{11}$) and 13dB in the second one ($\omega > \omega_{01}$).

A better EMI reduction is reachable with the selection of a better appropriated map and a larger modulation index m.

VII. Conclusions

Spread spectrum technique is an efficient method to reduce the EMI spectrum of mixed signal circuits. Its special feature is the realisation without power devices (like required for EMI filters) and hence the fully integrability on chip. We proposed systems for

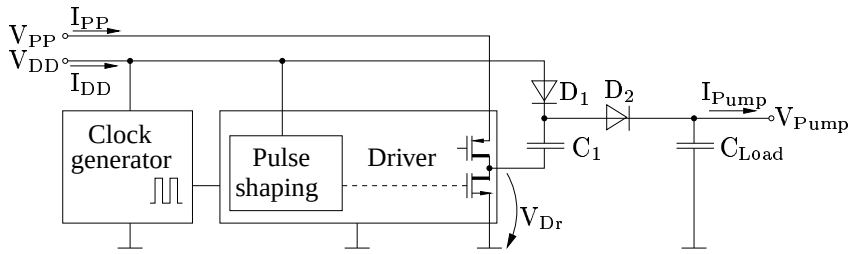

Fig. 19. Single stage charge pump

chaotic clock generation and PFM. Chaotic clock generation basing on the system depicted in Fig. 9 requires a nonlinear map. The improvement in EMI strongly depends on the map and hence the election of an appropriated map is an important step in the design of these systems. Schematics of piecewise linear maps were shown.

Further investigation will conentrate on efficient spectrum calculation and system level description of mixed signal circuits, especially switched power supplies.

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