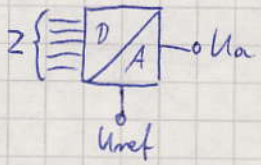
D/A- und A/D-Wandler

D/A-Wandler

Prinzip



$U_a = U_{LSB} \cdot Z = \frac{U_{ref}}{2^n} \cdot Z$

→ Folie
- 3/8 wird nicht erreicht
- MSB ... most significant Bit
- LSB ... least significant Bit

Charakterisierung und Fehler

a) Kenndaten

Wortbreite / Auflösung in Bit: $\Delta U_a = U_{LSB} = \frac{U_{ref}}{2^n}$

Wandlergeschwindigkeit in S/s

b) Bewertung von statischen Fehlern Quelle: Seifart

- absolute Linearität - max. Abweichung von der idealen Kennlinie

$$ANL = \left| \frac{U_z - U_0}{U_{LSB}} - Z \right|_{max} \qquad 0 \le Z < 2^n$$ → Folie

(englisch-sprachig Literatur „integral linearity", INL)

- integrale Linearität - max. Abweichung von der „besten" linearen Kennlinie → englisch: „best line linearity"

- „beste" Kennlinie: lineare Kennlinie durch die Messpunkte so, dass $\sum_1^n (U_n - U_{Lin})^2 \to min$ (least square fit)

- Endpunkt-Linearität - max. Abweichung von einer Geraden, die durch U_0 und $U_{Full\,scale}$ geht

- Differentielle Linearität

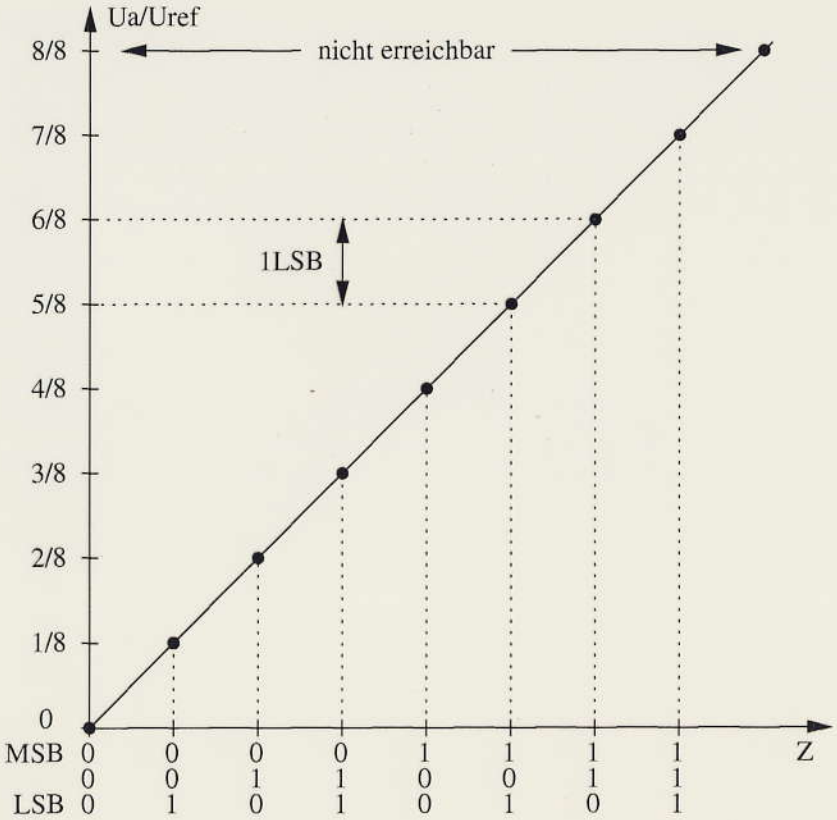
$$DNL = \left| \frac{U_{z+a} - U_z}{U_{LSB}} - 1 \right|_{max} \qquad 0 \le Z < 2^{n-1}$$

- max. Abweichung der Stufenhöhe vom Idealwert

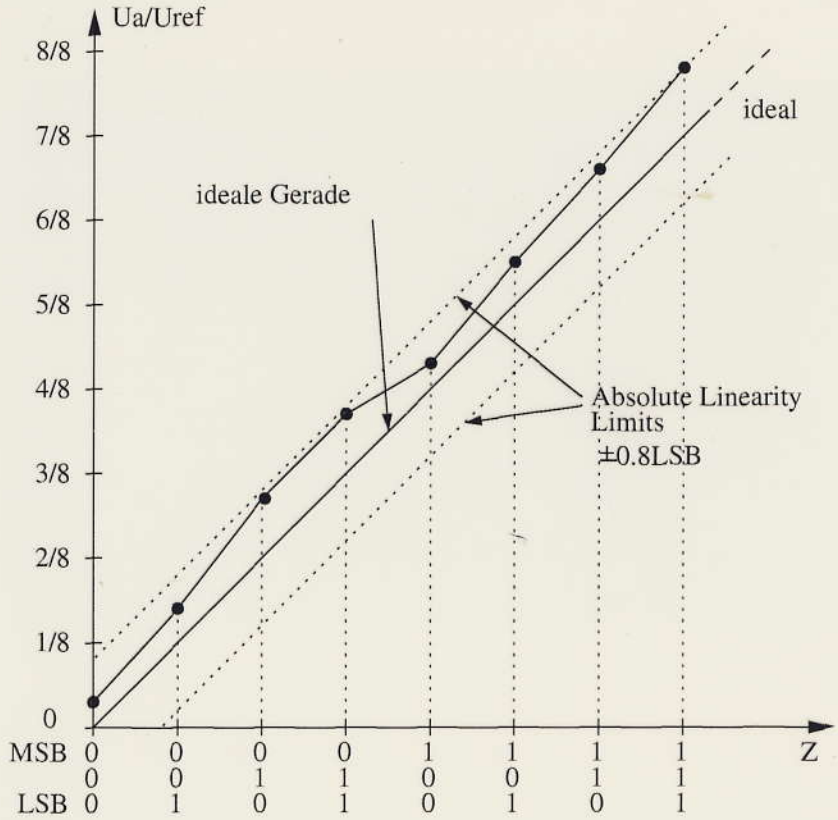
- Monotoniefehler

- tritt bei $\Delta U < 0$ auf
- sollte nicht vorkommen

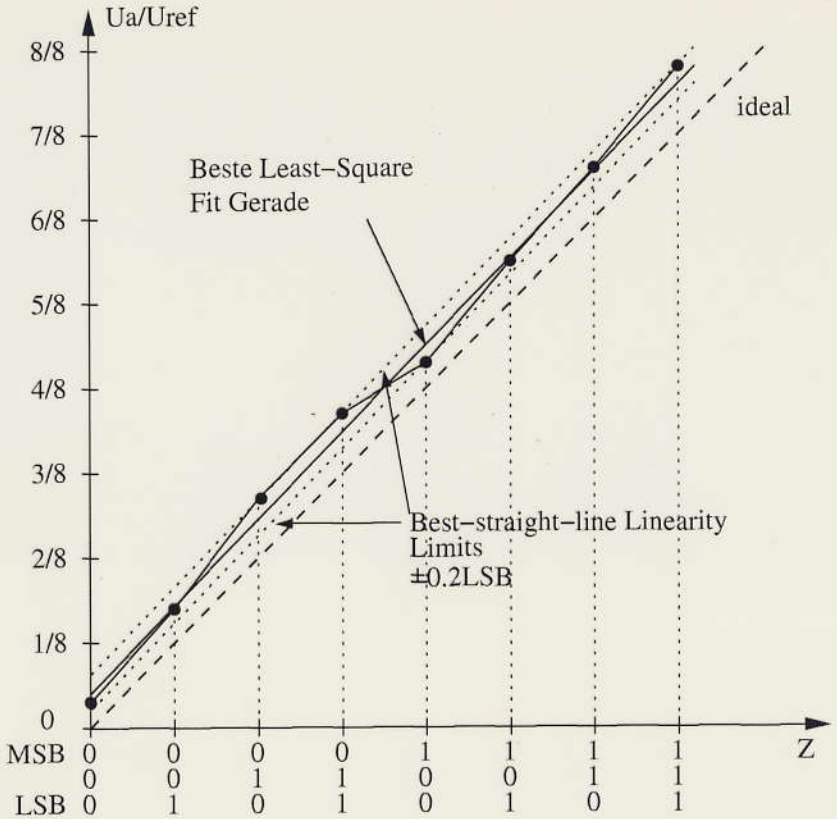
Ideale Kennlinie eines 3Bit-Wandlers



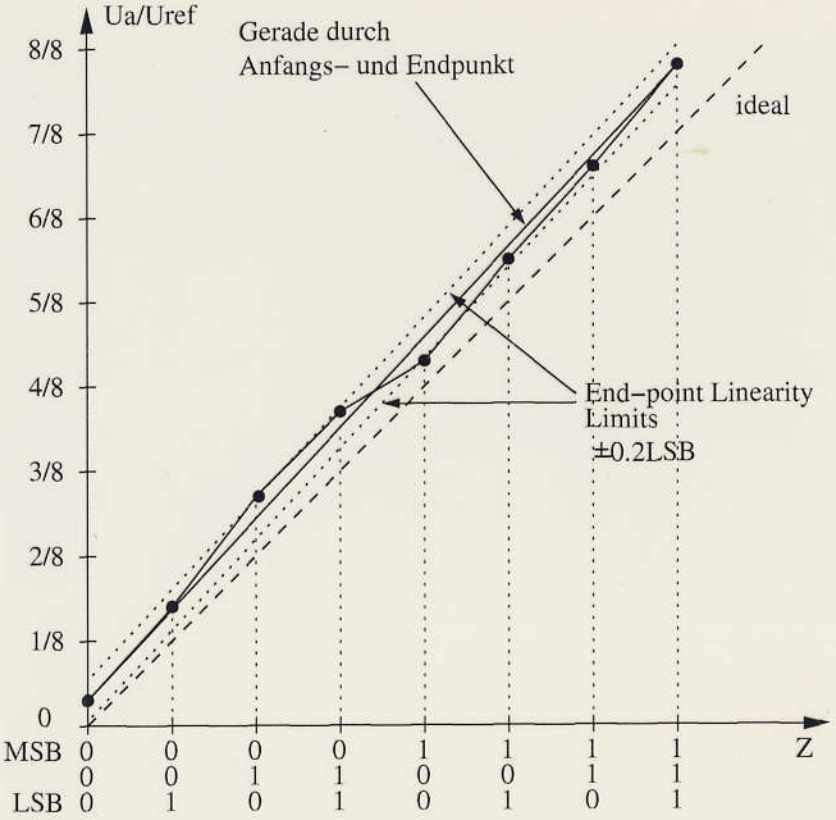
Absolute Linearität



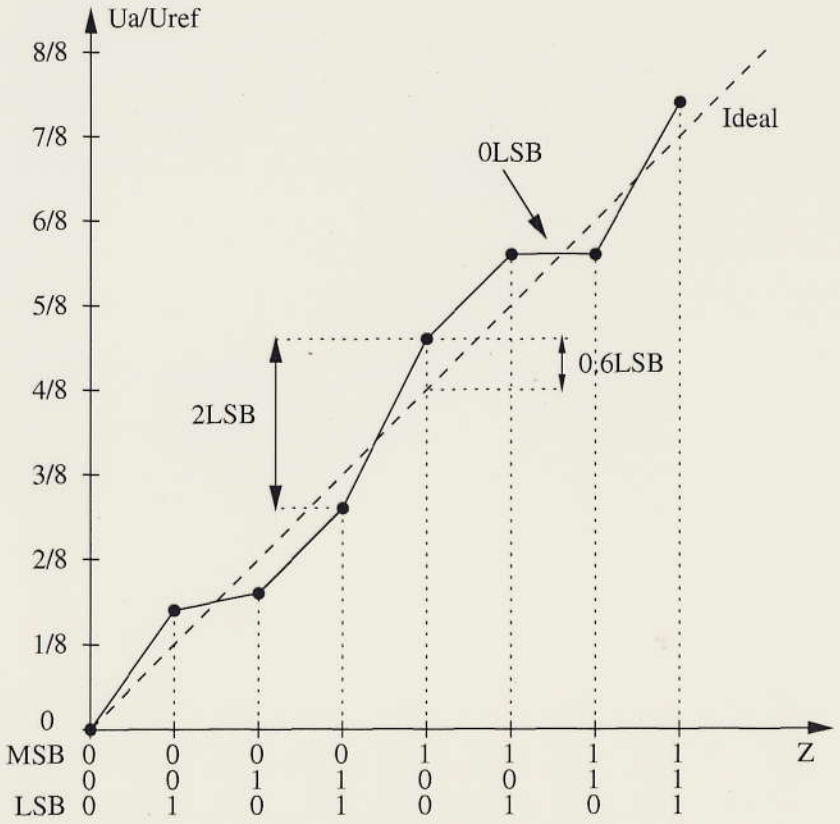
Best-Line (integrale) Lin.



Endpunkt Linearität

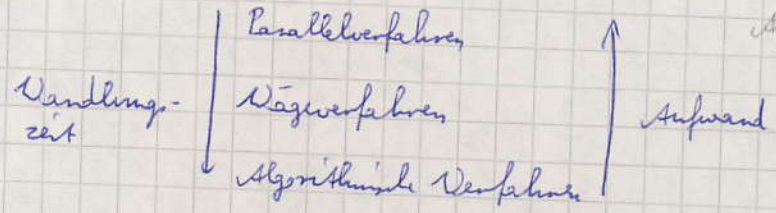


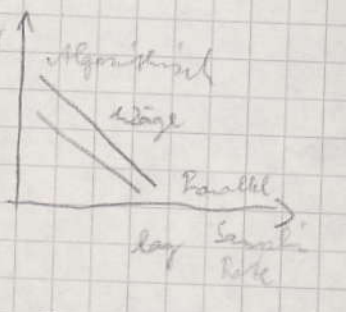
0.6LSB integrale Linearität und 1LSB differentielle Linearität



Realisierung

Verfahren




Auflösung log
Algorithmisch
Wäge
Parallel
log Samp. Rate

a) Parallelverfahren / Thermometer-Codewandler

Folie
- immer nur 1 Schalter geschlossen
- 2^N Schalter notwendig
- selten angewandt

Auflösung · Wandlungsrate $\hat{=}$ Technologiekonstante

b) Wägeverfahren

Folie - Summation gewichteter Ströme mit N Umschaltern

$$U_a = -\frac{R}{R_x} \cdot U_{ref} = -U_{ref}\left(\frac{1}{16}Z_0 + \frac{1}{8}Z_1 + \frac{1}{4}Z_2 + \frac{1}{2}Z_3\right)$$

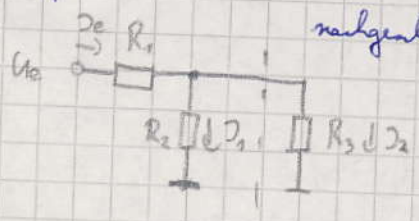
$$U_a = 0 \ldots -\frac{15}{16}U_{ref}$$

- Problem aufwändiges Widerstandsnetzwerk (matching) $R, 2R, 4R, 8R, \ldots$

Realisierung mit R-2R Netzwerk → Folie

- Summation gewichteter Ströme wie bei Wägeverfahren

Prinzip:



Forderung: $I_1 = \frac{1}{2} I_e$

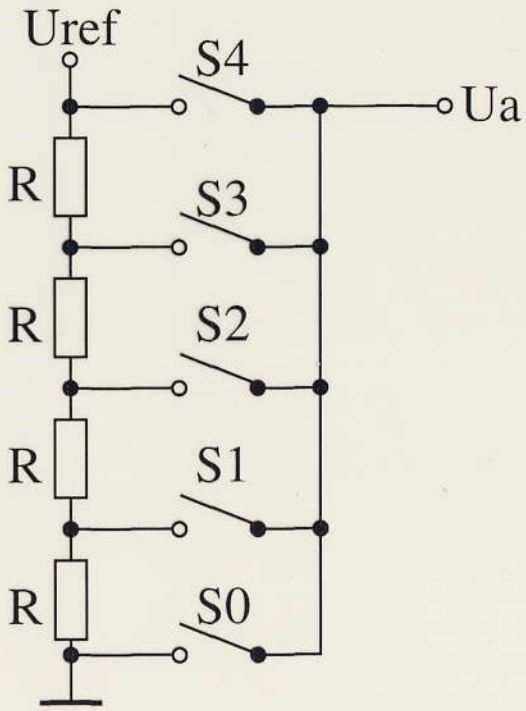
$I_2 = \frac{1}{2} I_e$ ($\hat{=} I_e$ der nachgeschalteten Stufe)

↳ $R_3 = R_2$

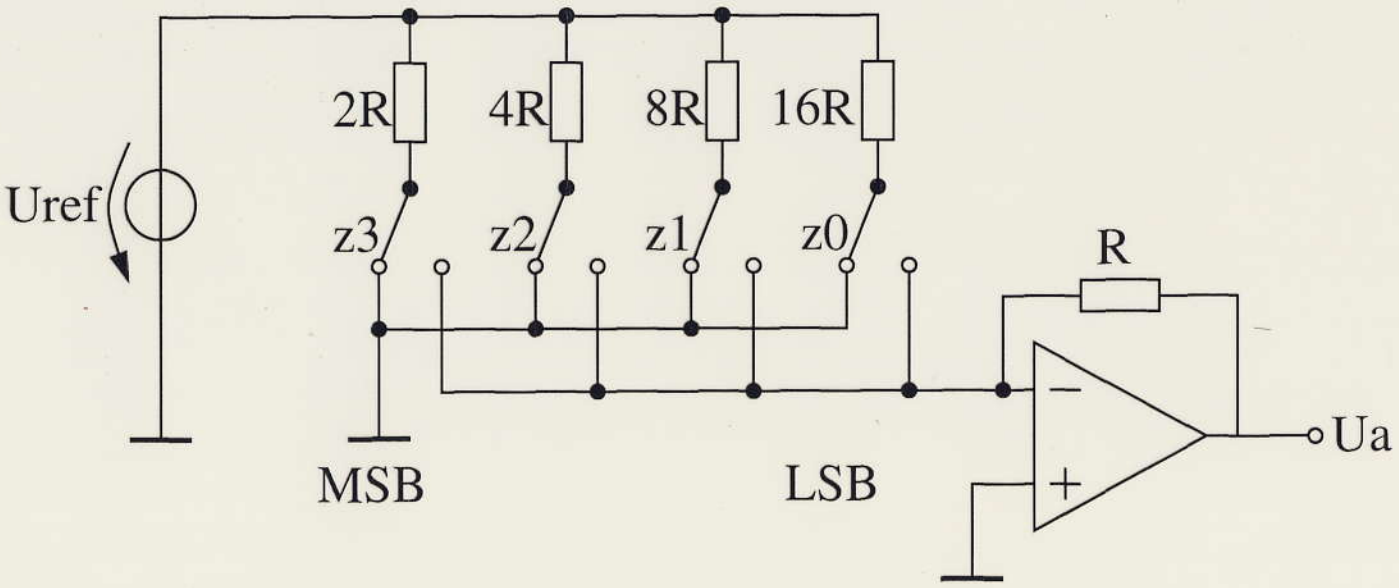
Ankopplung der nachgeschalteten Stufe an die vorherige:

$R_3 \hat{=} R_1 + \frac{R_2}{2} \equiv R_2 \rightarrow R_1 = \frac{1}{2} R_2$

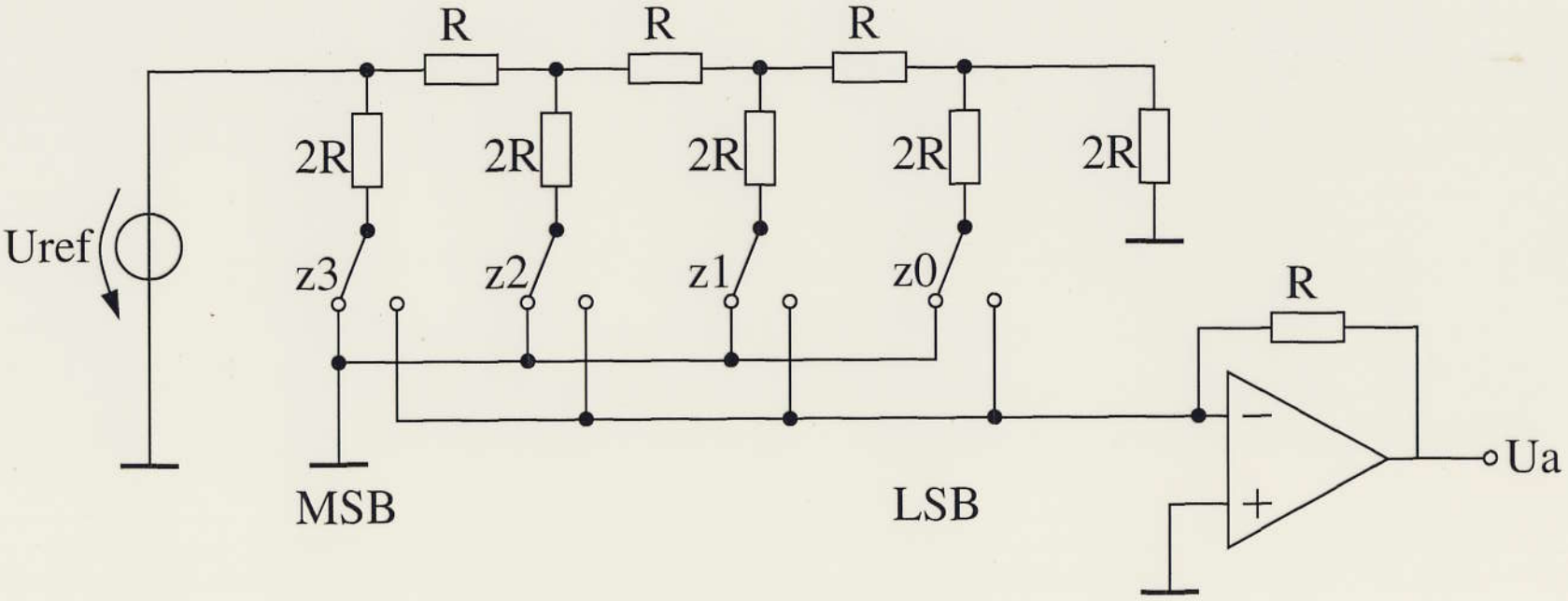
Parallelverfahren



Wägeverfahren



Realisierung mit R–2R–Netzwerk



- Geschaltete Stromquellen

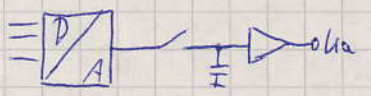
Folie
- für U_{BE} = konst. Dimensionierung der Widerstände wie R-2R-Realisierung
- Transistorflächen auf $\frac{1}{2}$, $\frac{1}{4}$... dimensioniert, wegen $U_{BE} = U_T \ln(\dots)$ ist matching weniger kritisch

Folie DAC0800

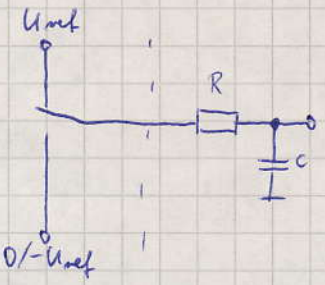
Problem des Wägeverfahrens: Glitches während der Umschaltvorgänge

Ursache: nicht synchrones Schalten der Schalter

Abhilfe: Track-and-Hold-Stufe am Ausgang



c) Algorithmische Wandler



Modulator Tiefpass (Mittelwertbildung)

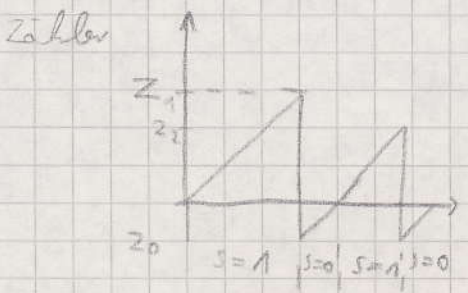
Schaltfrequenz $\gg$ Signalfrequenz → Oversampling D/A-Wandler

1 Schalter → 1 Bit-Wandler

Modulation z.B. PWM mit Zähler

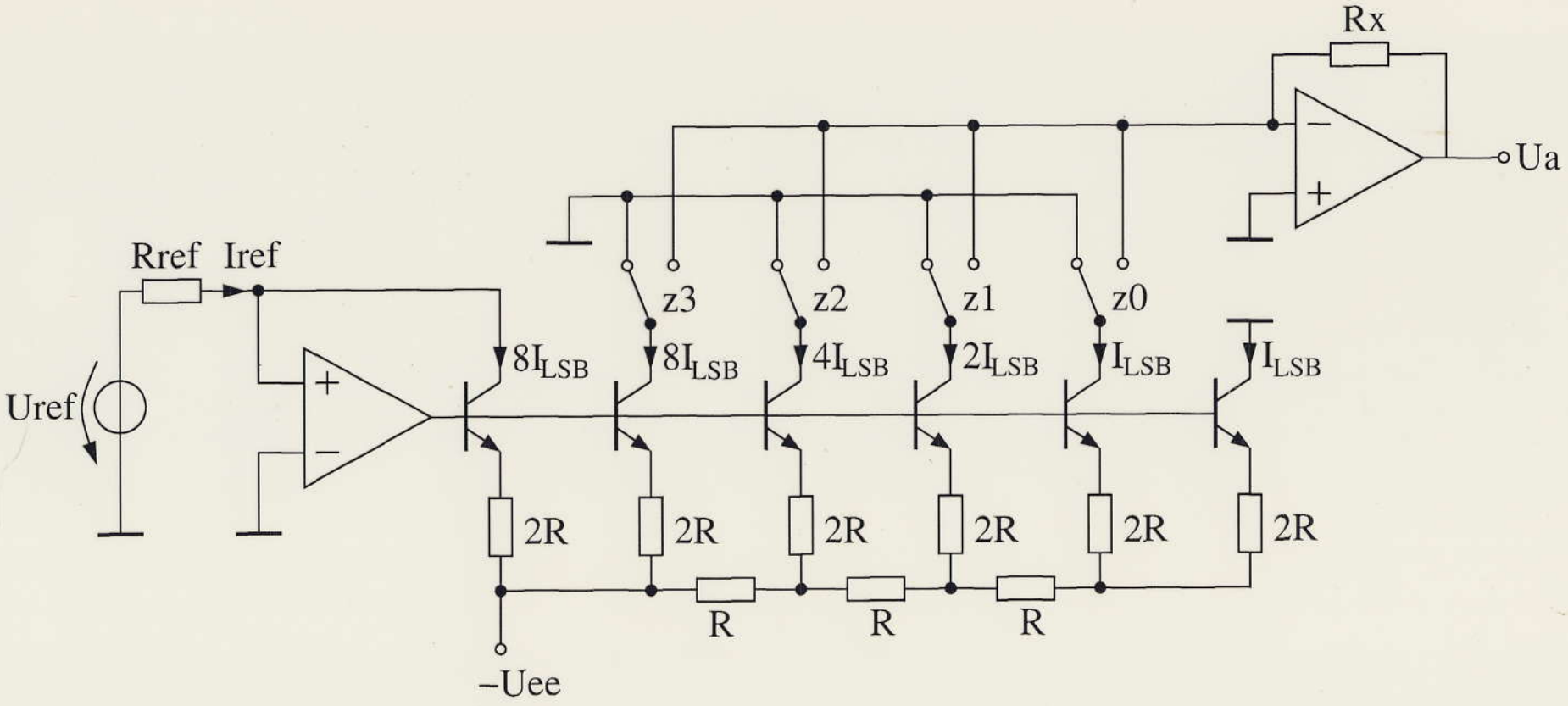
Folie Atmel $Z_0 + Z_e$ = konst.

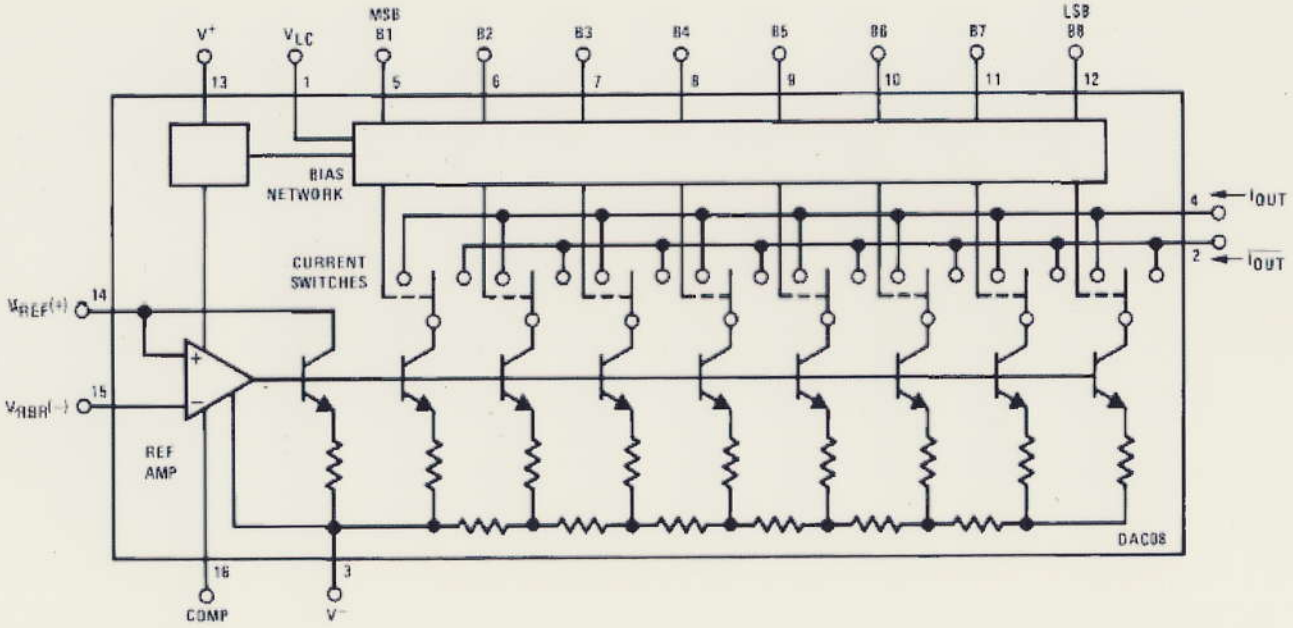
PFM:



Z_0 = konst, $Z_e = Z_x$

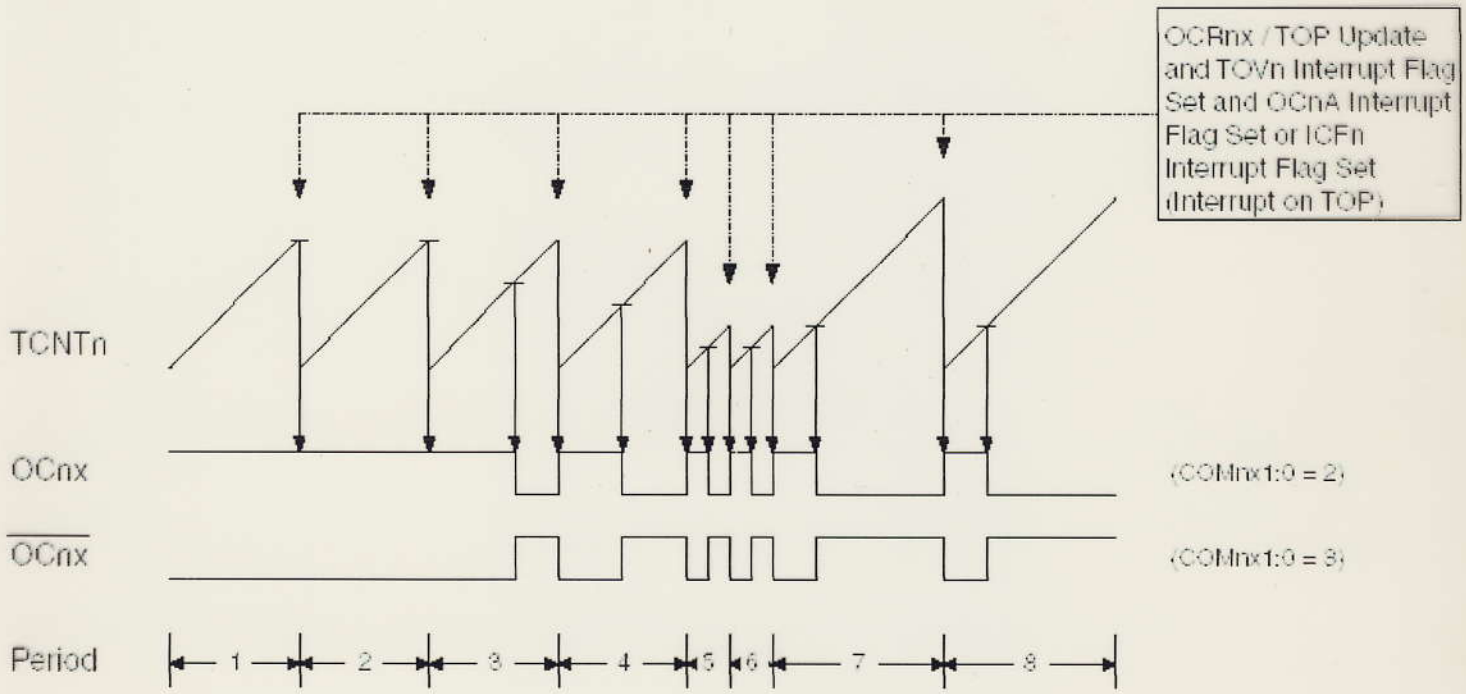
Realisierung mit geschalteten Stromquellen

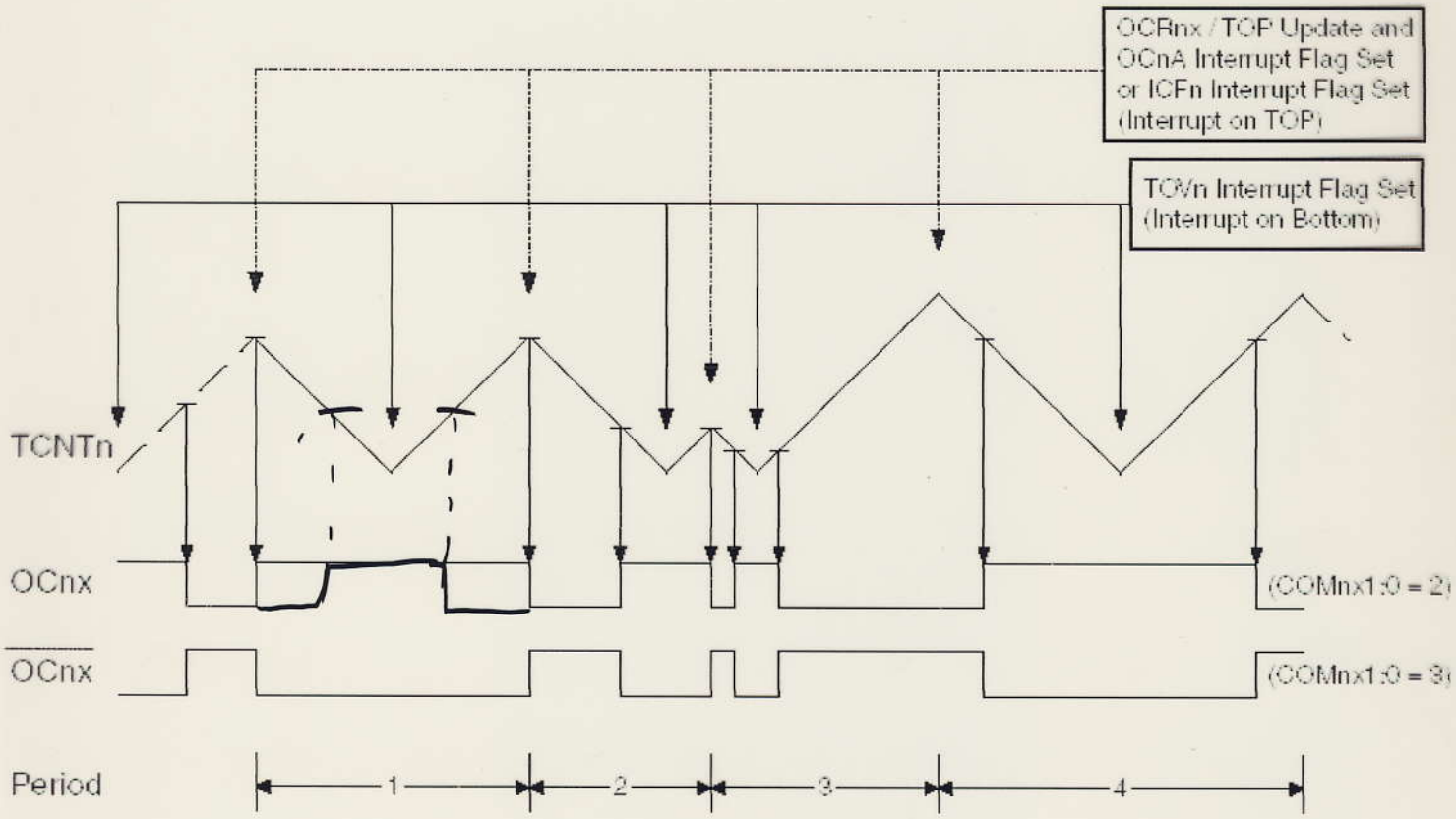




Block– und Prinzipschaltung
DAC0800 (Maxim)

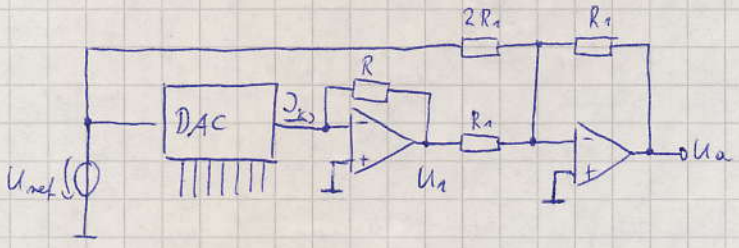
Pulsweitenmodulation (Atmega8), Atmel





Anwendungen

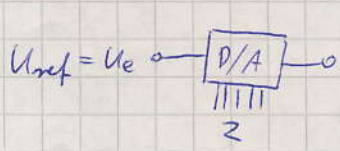
- Bipolares Ausgangssignal



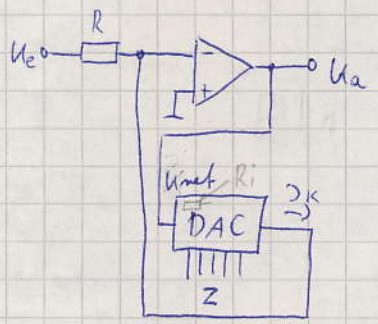
$$U_1 = -R I_k$$

$$U_a = -R_1\left(\frac{U_1}{R_1} + \frac{U_{ref}}{2R_1}\right) = I_k R - \frac{1}{2}U_{ref}$$

- Multiplizierender D/A-Wandler



- Dividierender D/A-Wandler



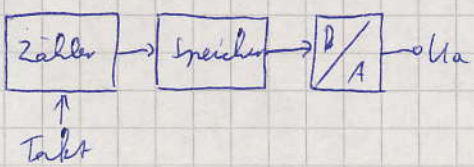
$$-\frac{U_e}{R} = \frac{Z}{2^n} \cdot \frac{U_a}{R_i}$$

$$U_a = -\frac{U_e}{Z} \cdot \frac{R_i}{R} \cdot 2^N$$

- Lautstärkeregler
- Mischen von Signalen

- Funktionsgenerator

Erzeugung periodischer Signale



19-1315; Rev 1; 12/97

MAXIM

Low-Power, Dual, 10-Bit, Voltage-Output DACs with Serial Interface

General Description

The MAX5158/MAX5159 low-power, serial, voltage-output, dual, 10-bit digital-to-analog converters (DACs) consume only 500µA from a single +5V (MAX5158) or +3V (MAX5159) supply. These devices feature Rail-to-Rail® output swing and are available in a space-saving 16-pin QSOP package. To maximize dynamic range, the DAC output amplifiers are configured with an internal gain of +2V/V.

The 3-wire serial interface is SPI™/QSPI™ and Microwire™ compatible. Each DAC has a double-buffered input organized as an input register followed by a DAC register, which allows the input and DAC registers to be updated independently or simultaneously with a 16-bit serial word. Additional features include a 2µA programmable shutdown, hardware-shutdown lockout, a separate reference-voltage input for each DAC that accepts AC and DC signals, and an active-low clear input ($\overline{CL}$) that resets all registers and DACs to zero. The MAX5158/MAX5159 provide a programmable logic pin for added functionality and a serial-data output pin for daisy chaining.

Applications

Digital Offset and Gain Adjustment

µP-Controlled Systems

Motion Control

Remote Industrial Controls

Features

- ♦ **10-Bit Dual DAC with Internal Gain of +2V/V**
- ♦ **Rail-to-Rail Output Swing**
- ♦ **8µs Settling Time**
- ♦ **Single-Supply Operation: +5V (MAX5158)**
  +3V (MAX5159)
- ♦ **Low Quiescent Current: 500µA (normal operation)**
  2µA (shutdown mode)
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **Available in Space-Saving 16-Pin QSOP Package**
- ♦ **Power-On Reset Clears Registers and DACs to Zero**
- ♦ **Adjustable Output Offset**

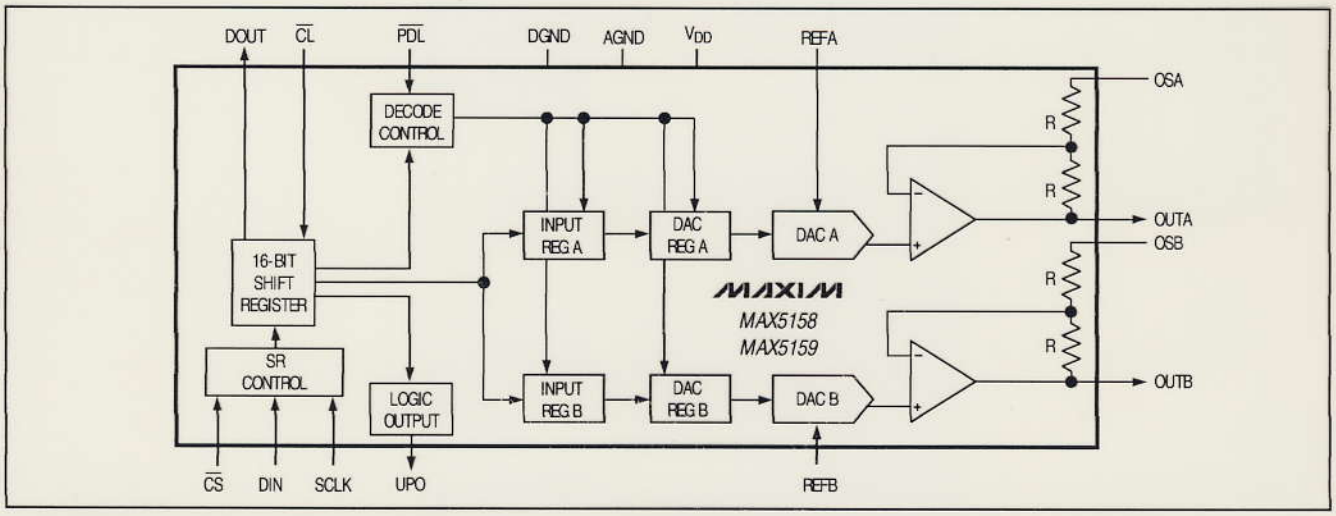
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX5158CPE	0°C to +70°C	16 Plastic DIP
MAX5158CEE	0°C to +70°C	16 QSOP
MAX5158EPE	-40°C to +85°C	16 Plastic DIP
MAX5158EEE	-40°C to +85°C	16 QSOP
MAX5158MJE	-55°C to +125°C	16 CERDIP*

Ordering Information continued at end of data sheet.

**Contact factory for availability.*

Functional Diagram



Rail-to-Rail is a registered trademark of Nippon Motorola Ltd. Microwire is a trademark of National Semiconductor Corp. SPI and QSPI are trademarks of Motorola, Inc.

Low-Power, Dual, 10-Bit Voltage-Output DACs with Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to +6V
V_{DD} to DGND .....-0.3V to +6V
AGND to DGND .....±0.3V
OSA, OSB to AGND .....(AGND - 4V) to (V_{DD} + 0.3V)
REF_, OUT_ to AGND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs (SCLK, DIN, $\overline{CS}$, $\overline{CL}$, PDL) to DGND .....(-0.3V to +6V)
Digital Outputs (DOUT, UPO) to DGND .....-0.3V to (V_{DD} + 0.3V)
Maximum Current into Any Pin .....±20mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.5mW/°C above +70°C) 842mW
QSOP (derate 8.30mW/°C above +70°C) 667mW
CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges
MAX515_C_E .....0°C to +70°C
MAX515_E_E .....-40C° to +85°C
MAX515_MJE .....-55°C to +125°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX5158

(V_{DD} = +5V ±10%, V_{REFA} = V_{REFB} = 2.048V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A= +25°C (OS_ tied to AGND for a gain of +2V/V).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution			10			Bits
Integral Nonlinearity	INL	(Note 1)			±1	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Offset Error	$V_{OS\_}$	Code = 2			±6	mV
Offset Tempco	TCV_{OS}	Normalized to 2.048V		4		ppm/°C
Gain Error				-0.1	1	LSB
Gain-Error Tempco		Normalized to 2.048V		4		ppm/°C
V_{DD} Power-Supply Rejection Ratio	PSRR	2.7V ≤ V_{DD} ≤ 5.5V		20	260	µV/V
REFERENCE INPUT						
Reference Input Range	REF		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Minimum with code 1558 hex	18	25		kΩ
MULTIPLYING-MODE PERFORMANCE						
Reference 3dB Bandwidth		Input code = 1FF8 hex, $V_{REF\_}$ = 0.67Vp-p at 0.75V_{DC}		300		kHz
Reference Feedthrough		Input code = 0000 hex, $V_{REF\_}$ = (V_{DD} - 1.4 Vp-p) at 1kHz		-82		dB
Signal-to-Noise plus Distortion Ratio	SINAD	Input code = 1FF8 hex, $V_{REF\_}$ = 1Vp-p at 1.25V_{DC}, f = 25kHz		75		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}	$\overline{CL}$, $\overline{PDL}$, $\overline{CS}$, DIN, SCLK	3			V
Input Low Voltage	V_{IL}	$\overline{CL}$, $\overline{PDL}$, $\overline{CS}$, DIN, SCLK			0.8	V
Input Hysteresis	V_{HYS}			200		mV
Input Leakage Current	I_{IN}	V_{IN} = 0V to V_{DD}		0.001	±1	µA
Input Capacitance	C_{IN}			8		pF

Low-Power, Dual, 10-Bit Voltage-Output DACs with Serial Interface

ELECTRICAL CHARACTERISTICS—MAX5159

(V_{DD} = +2.7V to +3.6V, V_{REFA} = V_{REFB} = 1.25V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C (OS_ pins tied to AGND for a gain of +2V/V).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution			10			Bits
Integral Nonlinearity	INL	(Note 5)			±1	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Offset Error	V_{OS}	Code = 3			±6	mV
Offset Tempco	TCV_{OS}	Normalized to 1.25V		6.5		ppm/°C
Gain Error				-0.1	±1	LSB
Gain-Error Tempco		Normalized to 1.25V		6.5		ppm/°C
V_{DD} Power-Supply Rejection Ratio	PSRR	2.7V ≤ V_{DD} ≤ 3.6V		40	320	µV/V
REFERENCE INPUT (VREF)						
Reference Input Range	REF		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Minimum with code 1558 hex	18	25		kΩ
MULTIPLYING-MODE PERFORMANCE						
Reference 3dB Bandwidth		Input code = 1FF8 hex, $V_{REF\_}$ = 0.67Vp-p at 0.75V_{DC}		300		kHz
Reference Feedthrough		Input code = 0000 hex, $V_{REF\_}$ = (V_{DD} - 1.4)Vp-p at 1kHz		-82		dB
Signal-to-Noise plus Distortion Ratio	SINAD	Input code = 1FF8 hex, $V_{REF\_}$ = 1Vp-p at 1V_{DC}, f = 15kHz		73		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}	$\overline{CL}$, $\overline{PDL}$, $\overline{CS}$, DIN, SCLK	2.2			V
Input Low Voltage	V_{IL}	$\overline{CL}$, $\overline{PDL}$, $\overline{CS}$, DIN, SCLK			0.8	V
Input Hysteresis	V_{HYS}			200		mV
Input Leakage Current	I_{IN}	V_{IN} = 0V to V_{DD}		0	±1	µA
Input Capacitance	C_{IN}			8		pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA		0.13	0.4	V
DYNAMIC PERFORMANCE (DOUT, UPO)						
Voltage Output Slew Rate	SR			0.75		V/µs
Output Settling Time		To 1/2LSB of full-scale, V_{STEP} = 2.5V		8		µs
Output Voltage Swing		Rail-to-rail (Note 6)		0 to V_{DD}		V
OSA or OSB Input Resistance	$R_{OS\_}$		24	34		kΩ
Time Required for Valid Operation after Shutdown				25		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, f_{DIN} = 100kHz, V_{SCLK} = 3Vp-p		5		nV-s
Digital Crosstalk				5		nV-s

Low-Power, Dual, 10-Bit, Voltage-Output DACs with Serial Interface

Pin Description

PIN	NAME	FUNCTION
1	AGND	Analog Ground
2	OUTA	DAC A Output Voltage
3	OSA	DAC A Offset Adjustment
4	REFA	Reference for DAC A
5	$\overline{CL}$	Active-Low Clear Input. Resets all registers to zero. DAC outputs go to 0V.
6	$\overline{CS}$	Chip-Select Input
7	DIN	Serial-Data Input
8	SCLK	Serial Clock Input
9	DGND	Digital Ground
10	DOUT	Serial-Data Output
11	UPO	User-Programmable Output
12	$\overline{PDL}$	Power-Down Lockout. The device cannot be powered down when $\overline{PDL}$ is low.
13	REFB	Reference for DAC B
14	OSB	DAC B Offset Adjustment
15	OUTB	DAC B Output Voltage
16	V_{DD}	Positive Power Supply

Detailed Description

The MAX5158/MAX5159 dual, 10-bit, voltage-output DACs are easily configured with a 3-wire serial interface. These devices include a 16-bit data-in/data-out shift register, and each DAC has a double-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition, trimmed internal resistors produce an internal gain of +2V/V that maximizes output voltage swing. The amplifier's offset-adjust pin allows for a DC shift in the DAC's output.

Both DACs use an inverted R-2R ladder network that produces a weighted voltage proportional to the input voltage value. Each DAC has its own reference input to facilitate independent full-scale values. Figure 1 depicts a simplified circuit diagram of one of the two DACs.

Reference Inputs

The reference inputs accept both AC and DC values with a voltage range extending from 0V to (V_{DD} - 1.4V). Determine the output voltage using the following equation (OS_ = AGND):

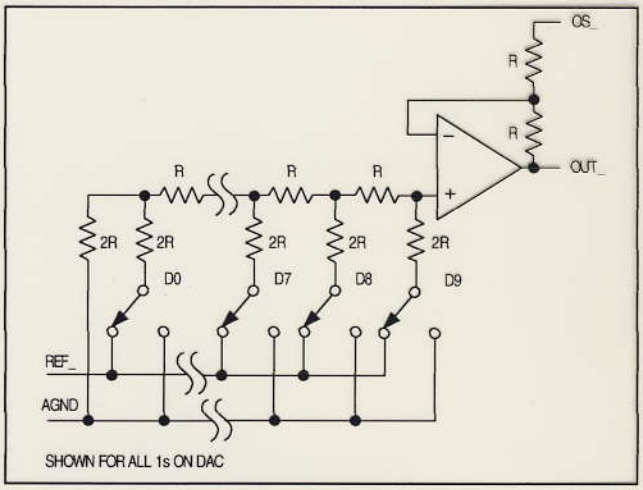


Figure 1. Simplified DAC Circuit Diagram

$$V_{OUT} = (V_{REF} \times NB / 1024) \times 2$$

where NB is the numeric value of the DAC's binary input code (0 to 1023) and V_{REF} is the reference voltage.

The reference input impedance ranges from 18kΩ (1558 hex) to several giga ohms (with an input code of 0000 hex). The reference input capacitance is code dependent and typically ranges from 15pF with an input code of all zeros to 50pF with a full-scale input code.

Output Amplifier

The output amplifiers on the MAX5158/MAX5159 have internal resistors that provide for a gain of +2V/V when OS_ is connected to AGND. These resistors are trimmed to minimize gain error. The output amplifiers have a typical slew rate of 0.75V/µs and settle to 1/2LSB within 8µs, with a load of 10kΩ in parallel with 100pF. Loads less than 2kΩ degrade performance.

The OS_ pin can be used to produce an adjustable offset voltage at the output. For instance, to achieve a 1V offset, apply -1V to the OS_ pin to produce an output range from 1V to (1V + V_{REF} x 2). Note that the DAC's output range is still limited by the maximum output voltage specification.

Power-Down Mode

The MAX5158/MAX5159 feature a software-programmable shutdown mode that reduces the typical supply current to 2µA. The two DACs can be shutdown independently, or simultaneously using the appropriate programming command. Enter shutdown mode by writing the appropriate input-control word (Table 1). In shutdown mode, the reference inputs and amplifier outputs become high impedance, and the serial interface

Table 2. Unipolar Code Table (Gain = +2)

DAC CONTENTS MSB LSB	ANALOG OUTPUT
11 1111 1111 (000)	$+V_{REF}\left(\frac{1023}{1024}\right) \times 2$
10 0000 0001 (000)	$+V_{REF}\left(\frac{513}{1024}\right) \times 2$
10 0000 0000 (000)	$+V_{REF}\left(\frac{512}{1024}\right) \times 2 = V_{REF}$
01 1111 1111 (000)	$+V_{REF}\left(\frac{511}{1024}\right) \times 2$
00 0000 0001 (000)	$+V_{REF}\left(\frac{1}{1024}\right)$
00 0000 0000 (000)	0V

Note: *( ) are for the sub bits.*

Serial-Data Output

The serial-data output, DOUT, is the internal shift register's output. DOUT allows for daisy chaining of devices and data readback. The MAX5158/MAX5159 can be programmed to shift data out of DOUT on SCLK's falling edge (Mode 0) or on the rising edge (Mode 1). Mode 0 provides a lag of 16 clock cycles, which maintains compatibility with SPI/QSPI and Microwire interfaces. In Mode 1, the output data lags 15.5 clock cycles. On power-up, the device defaults to Mode 0.

User-Programmable Logic Output (UPO)

UPO allows an external device to be controlled through the serial interface (Table 1), thereby reducing the number of microcontroller I/O pins required. On power-up, UPO is low.

Power-Down Lockout Input ($\overline{PDL}$)

The power-down lockout pin ($\overline{PDL}$) disables software shutdown when low. When in shutdown, transitioning $\overline{PDL}$ from high to low wakes up the part with the output set to the state prior to shutdown. $\overline{PDL}$ can also be used to asynchronously wake up the device.

Daisy Chaining Devices

Any number of MAX5158/MAX5159s can be daisy chained by connecting the DOUT pin of one device to the DIN pin of the following device in the chain (Figure 7).

Since the MAX5158/MAX5159's DOUT pin has an internal active pull-up, the DOUT sink/source capability determines the time required to discharge/charge a capacitive load. Refer to the digital output V_{OH} and V_{OL} specifications in the *Electrical Characteristics*.

Figure 8 shows an alternate method of connecting several MAX5158/MAX5159s. In this configuration, the data bus is common to all devices; data is not shifted through a daisy chain. More I/O lines are required in this configuration because a dedicated chip-select input ($\overline{CS}$) is required for each IC.

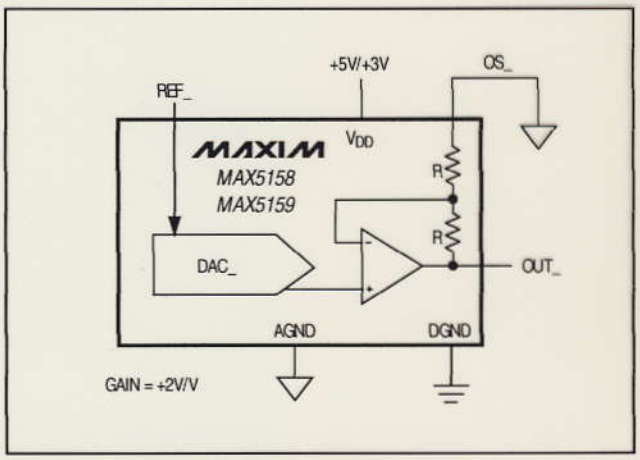


Figure 9. Unipolar Output Circuit (Rail-to-Rail)

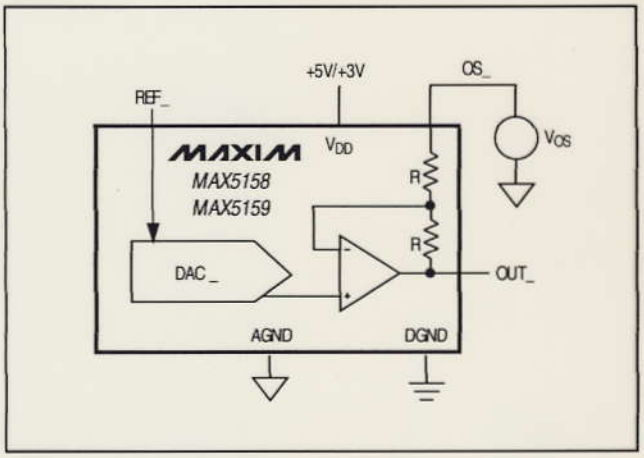


Figure 10. Setting OS_ for Output Offset

Applications Information

Unipolar Output

Figure 9 shows the MAX5158/MAX5159 configured for unipolar, rail-to-rail operation with a gain of +2V/V. The MAX5158 can produce a 0V to 4.096V output with a 2.048V reference (Figure 9), while the MAX5159 can