2. Verstärkerschaltungen

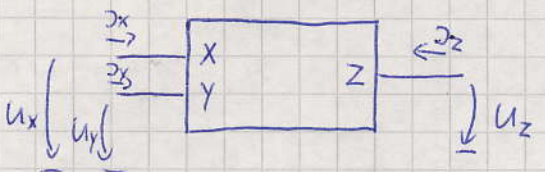
Klassifizierung nach Ein- und Ausgangsgrößen

Beschränkung auf einen Ausgang und (fast immer) einen Eingang

→ U, I , 4 Arten gesteuerter Quellen

eine wichtige Grundschaltung: Current Conveyor

2.1. Current Conveyor



2.1.1. CCI

$$\begin{pmatrix} I_y \\ U_x \\ I_z \end{pmatrix} = \begin{pmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{pmatrix} \cdot \begin{pmatrix} U_y \\ I_x \\ U_z \end{pmatrix}$$

CCI+ CCI-

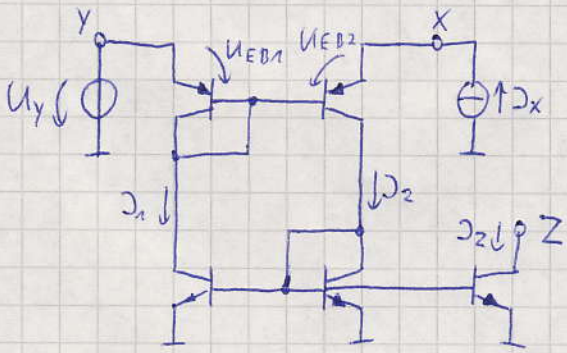
Ausgangsgrößen — Eingangsgrößen

X ... Stromeingang, Spannungsausgang

Y ... Spannungseingang, Stromausgang

Z ... Stromausgang

Realisierung:



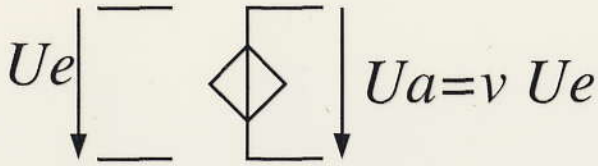
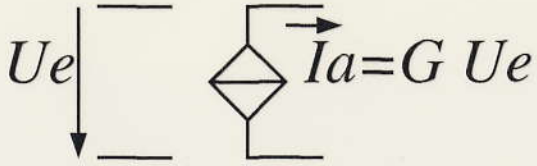
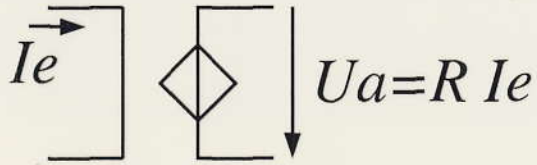
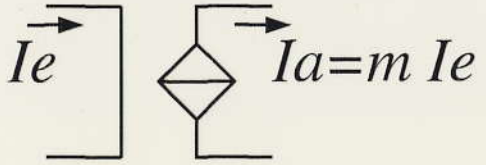
gleiche Transistoren

CCI+

$B \gg 1$: $I_1 = I_2$, $I_y = I_x \rightsquigarrow U_{EB1} = U_{EB2}$, $U_x = U_y$

$I_z = I_2 = I_x$ unabhängig von U_z

Nachteil / Problem: kein hochohmiger Spannungseingang vorhanden → CC II

Eingangsgröße	Ausgangsgröße: Spannung	Ausgangsgröße: Strom
Spannung	 Operationsverstärker Instrumentations–V.	 Transkonduktanz–V. OTA
Strom	 Transimpedanz–V. TIA	 Stromspiegel

2.1.2 CCII

$$\begin{pmatrix} I_Y \\ U_X \\ I_Z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{pmatrix} \begin{pmatrix} U_Y \\ I_X \\ U_Z \end{pmatrix}$$

CCII+ CCII-

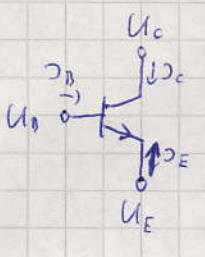
X ... Stromeingang Spannungsausgang

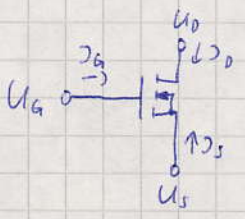
Y ... Spannungs~~ausgang~~ eingang

Z ... Stromausgang

$I_Y = 0$

Vergleich mit Bipolartransistor / FET



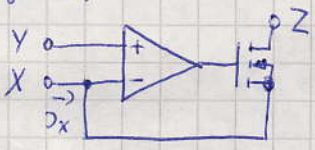


$B \to \infty$:

$I_B \to 0$	$B \to Y$		$I_G = 0$	$G \to Y$	
$I_C = -I_E$	$C \to Z$	CCII-	$I_D = -I_S$	$S \to X$	
$U_E = U_B - U_{BE}$	$E \to X$		$U_S = U_G - U_{GS}$	$D \to Z$	

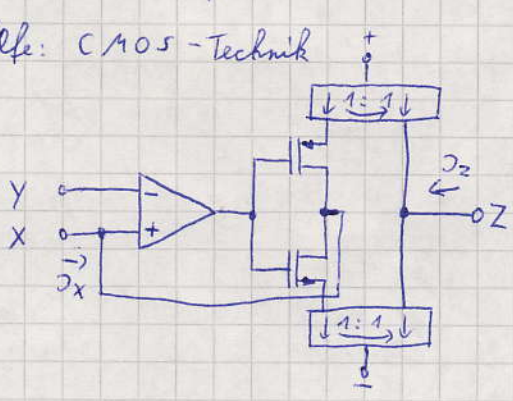
Fehler

Verringerung des Fehlers z. B. durch OPV

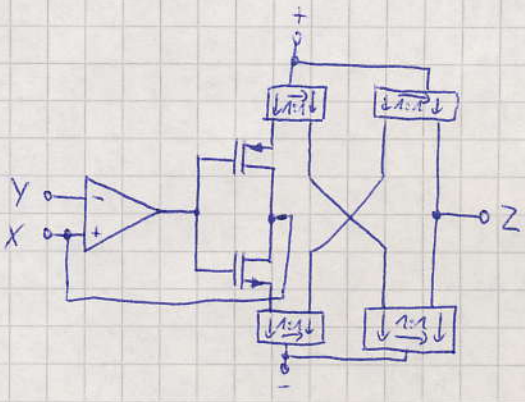


diese Schaltungen funktionieren nur für $U_Z > U_X, U_Y$

Abhilfe: CMOS-Technik



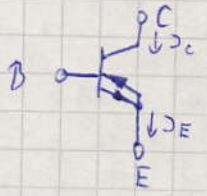
CCII+



CCII-

2.1.3. Realisierung durch OCs

~~Diamond~~ - Transistor



$I_B = 0$, $B \to \infty$
$U_{BE} = 0$
U_c beliebig
$I_c = I_E$

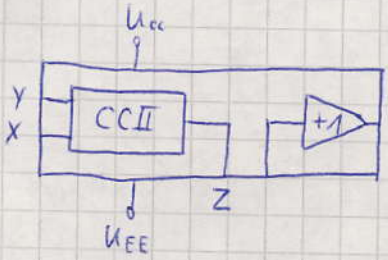
normaler Transistor

siehe vorheriges Blatt

Vorstellung eines idealen Transistors als CCII -

a) OPA 660

Aufbau



Diamond Transistor

Puffer

Folie Struktur, Funktion erklären

Anwendung: z.B. Breitbandverstärker (hohe Bandbreite)

Folie Anwendung

Bezeichnung OTA nur dann richtig, wenn mit Y gesteuert wird und an X Widerstand liegt, dann: $I_Z = U_X / R$

b) MAX 435 - Folie

enthält 2 CCII

$V_{in+} \triangleq Y$
$Z+ \triangleq X$
$IOUT+ \triangleq Z$

Anwendung folgt

auch hier hohe Bandbreite, siehe Oszillogramm

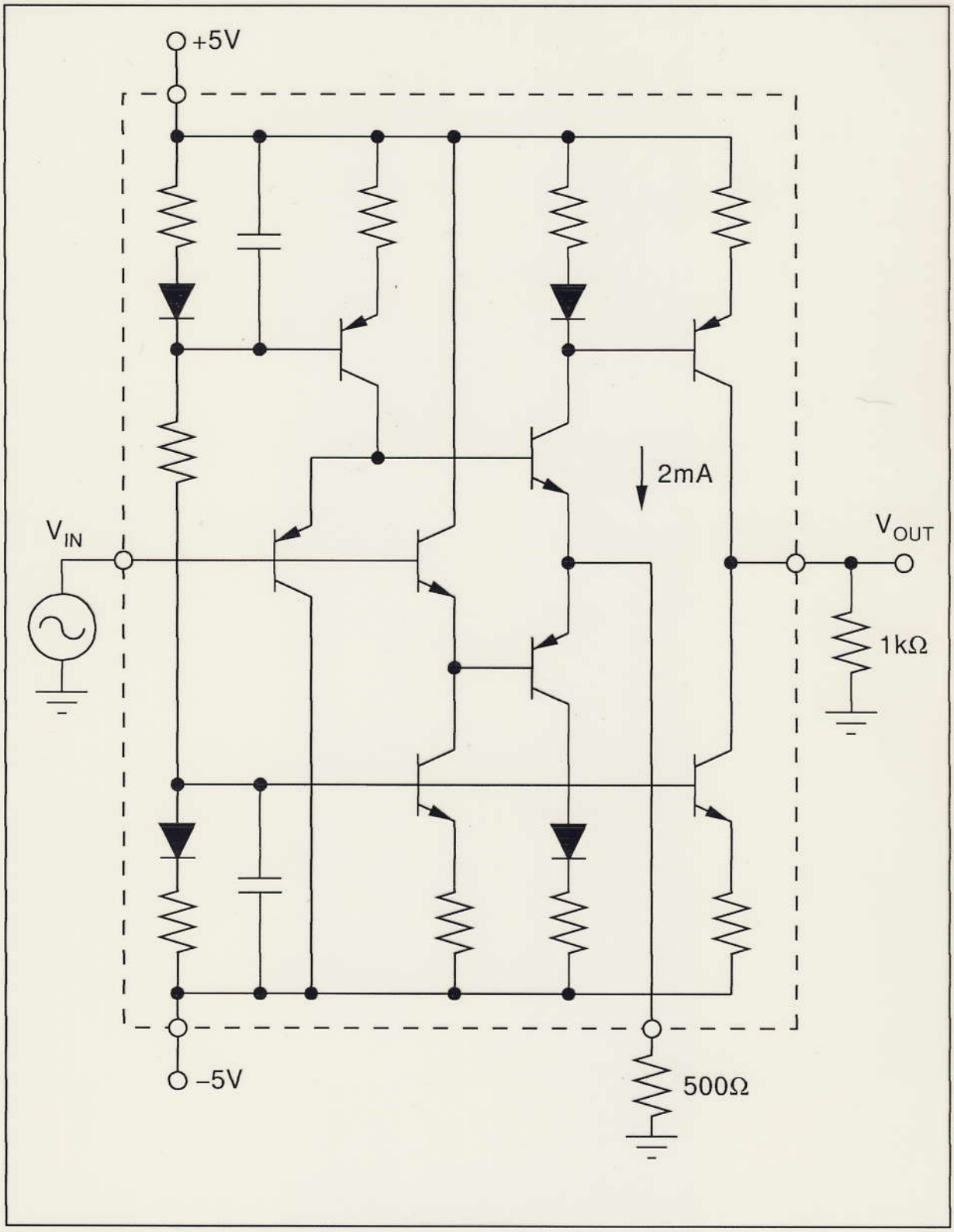
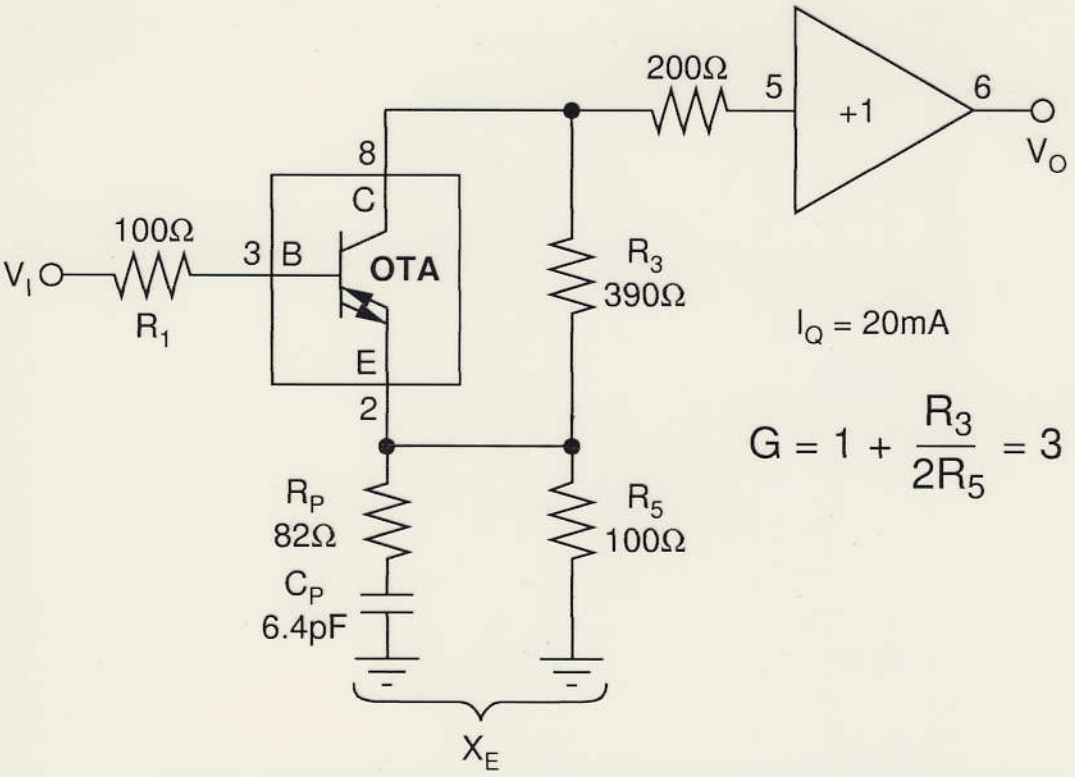
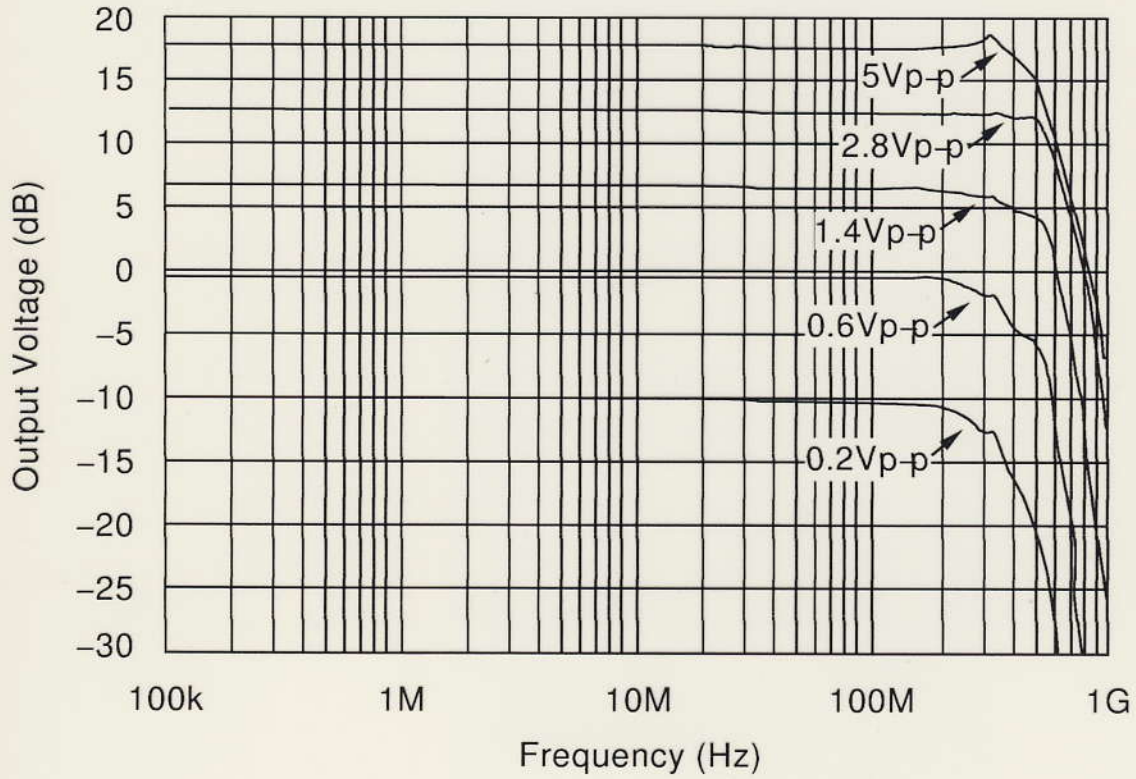
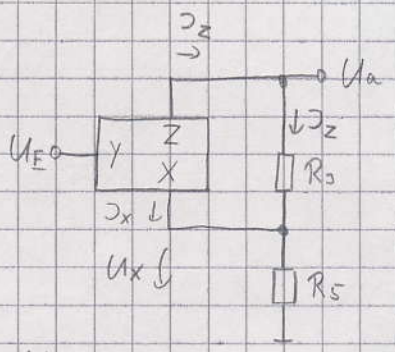


FIGURE 6. Diamond Structure.



OPA660 DIRECT-FEEDBACK FREQUENCY RESPONSE



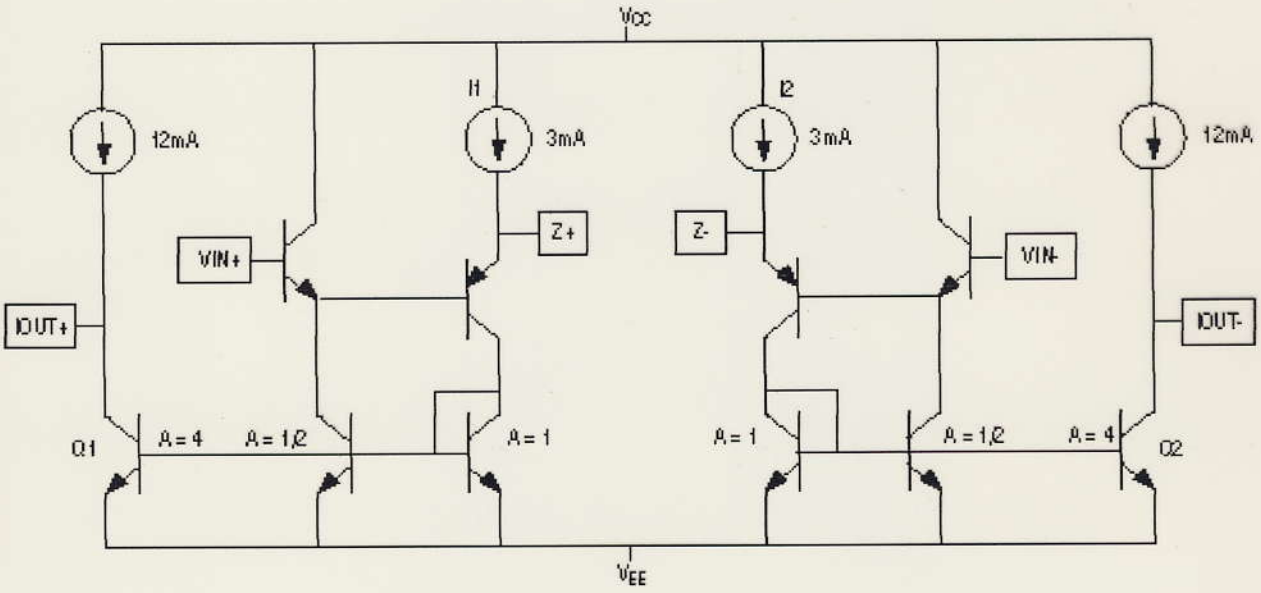


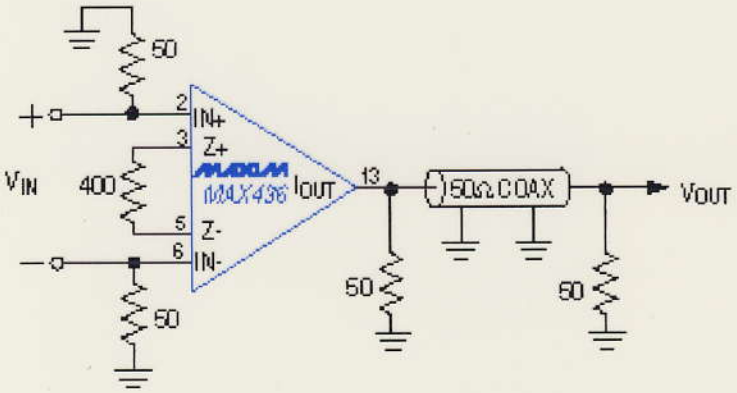
$U_x = U_E$

$U_x = (I_z + I_x) \cdot R_5$

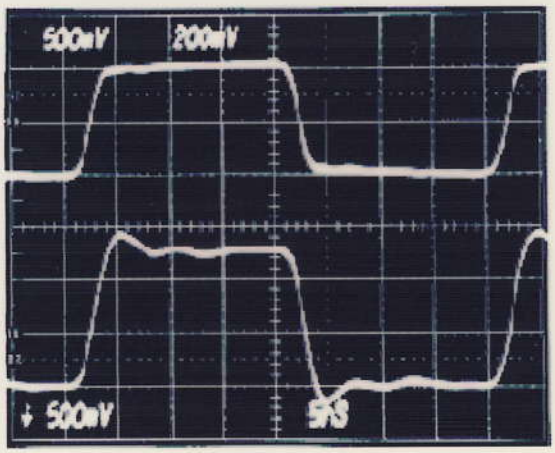
$I_x = I_z \rightarrow \quad I_z = \frac{U_E}{2R_5}$

$U_a = U_x + I_z R_3 = \quad U_E + U_E \frac{R_3}{2R_5}$





a.

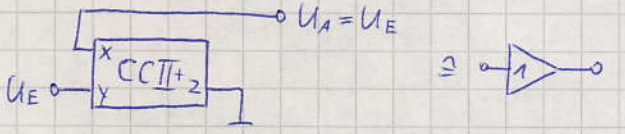


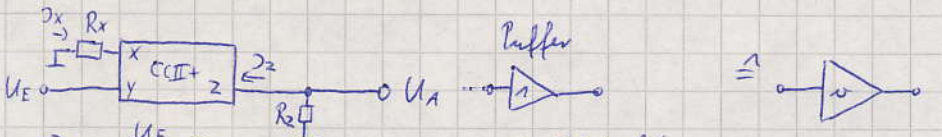
TIME (ns) 5ns/div
$R_t = 400\Omega$ $R_L = 25\Omega$

b.

2.1.4. CCII Anwendungen

a) Spannungsgesteuerte Spannungsquellen (Verstärker)



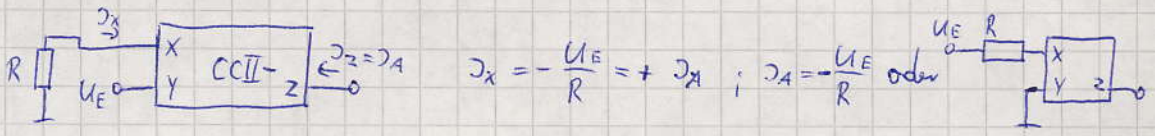


$J_X = -\frac{U_E}{R_X} = J_Z$ → 1 OPA 660

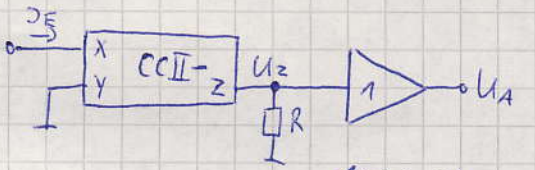
$U_a = -J_Z R_2 = U_E \cdot \underbrace{\frac{R_2}{R_X}}_{v}$

$r_a = R_2$ → Puffer erforderlich

b) Spannungsgesteuerte Stromquellen / OTA



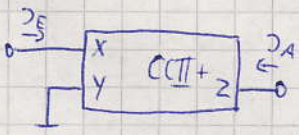
c) Stromgesteuerte Spannungsquellen / TIP



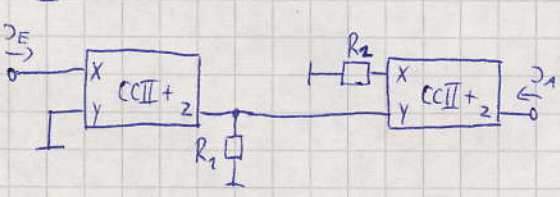
$U_A = U_Z = J_E \cdot R$

→ 1 OPA 660

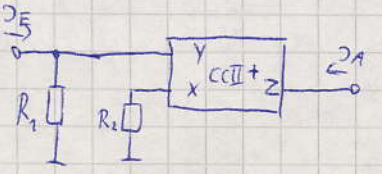
d) Stromgesteuerte Stromquellen



$J_A = J_E$, $U_E = 0$



$U_{R1} = -J_E \cdot R_1$; $J_A = -\frac{U_{R1}}{R_2} = J_E \cdot \frac{R_1}{R_2}$ $U_E = 0$

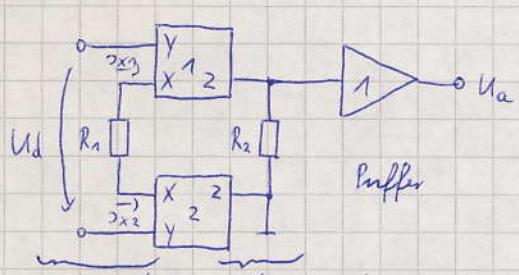


$U_y = U_x = J_E \cdot R_1$

$J_A = -\frac{U_x}{R_2} = -J_E \frac{R_1}{R_2}$

e) Instrumentationsverstärker

Verstärkung einer Differenzspannung



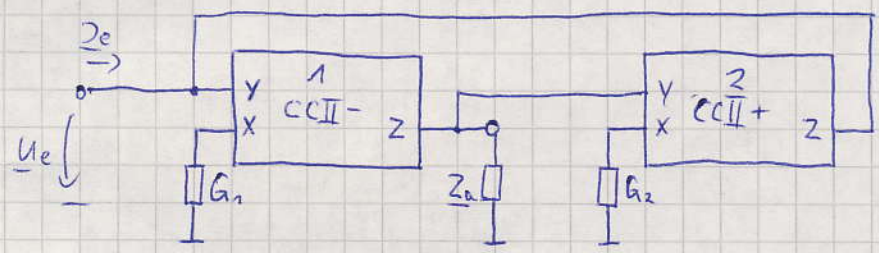
alles CCII+

$I_{x1} = -I_{x2} = -U_d / R_1$

$I_{z1} = I_{x1}, \quad U_{z1} = -I_{x1} \cdot R_2 = U_d \frac{R_2}{R_1} = U_a$

Folie FPAA

f) Gyrator

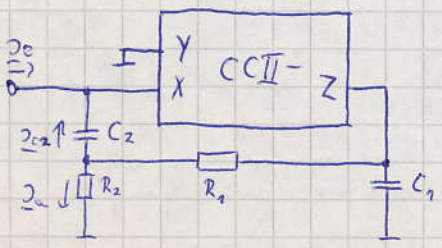


$\underline{U}_{z1} = -\underline{U}_e G_1 \underline{Z}_a \qquad \underline{Z}_e = \frac{\underline{U}_e}{\underline{I}_e} = \frac{1}{G_1 G_2 \underline{Z}_a}$

$\underline{I}_{z2} = -\underline{U}_{z1} G_2 = \underline{I}_e$

An A angeschlossene Kapazität wirkt am Eingang als Spule

g) Tiefpass 2. Ordnung in Stromtechnik



$\underline{U}_x = \underline{U}_y = 0 \rightarrow R_2 \parallel \frac{1}{sC_2}$

$\underline{I}_{c2} = sC_2 \underbrace{R_2 \cdot \underline{I}_a}_{\underline{U}_{c2}}$

$\underline{I}_x = \underline{I}_e + \underline{I}_{c2} = -\underline{I}_z = +\underline{I}_e + sC_2 R_2 \underline{I}_a$

$-\underline{I}_z = \underline{I}_a + \underline{I}_{c2} + sC_1 \left(\underline{I}_a R_2 + (\underline{I}_a + \underline{I}_{c2}) R_1 \right)$

$$\underline{U}_e + sC_2R_2\underline{U}_a = \underline{U}_2 + sC_2R_2\underline{U}_a + sC_1(\underline{U}_a R_2 + (\underline{U}_a + sC_2R_2\underline{U}_a)R_1)$$

$$\underline{U}_e = \underline{U}_a\,(1 + sC_1(R_1+R_2) + s^2C_1C_2R_1R_2)$$

$$\underline{G}(s) = \frac{1}{1 + sC_1(R_1+R_2) + s^2C_1C_2R_1R_2}$$

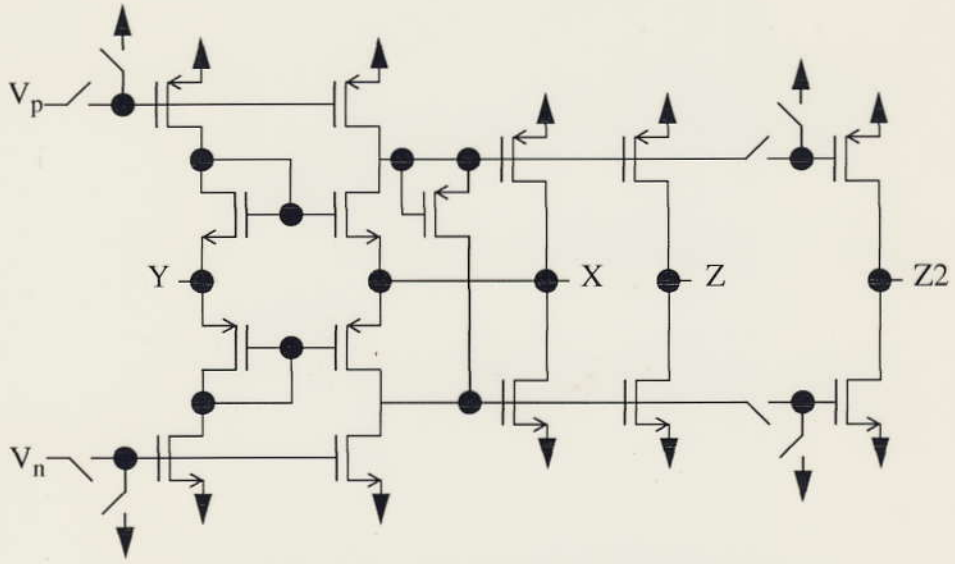


Figure 1: Current conveyor design including programming switches

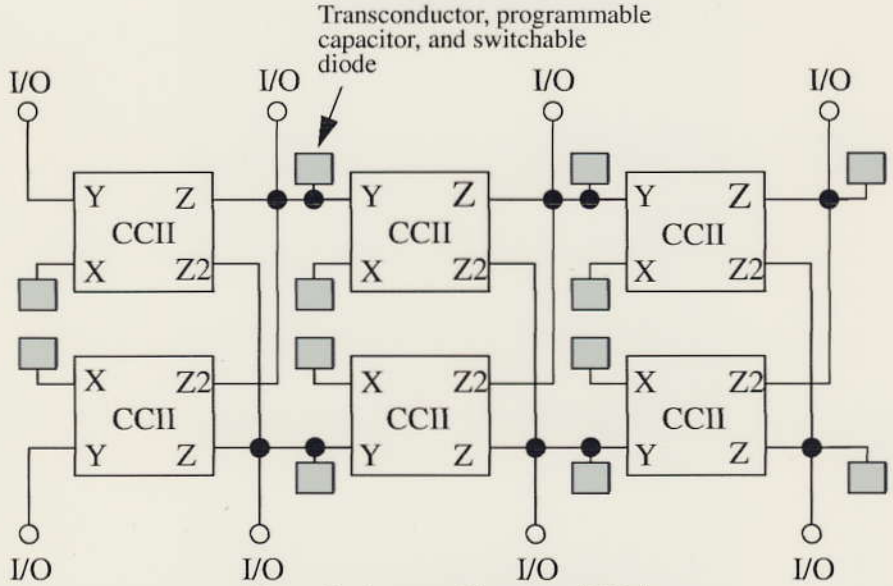


Figure 2: Array architecture of FPAA

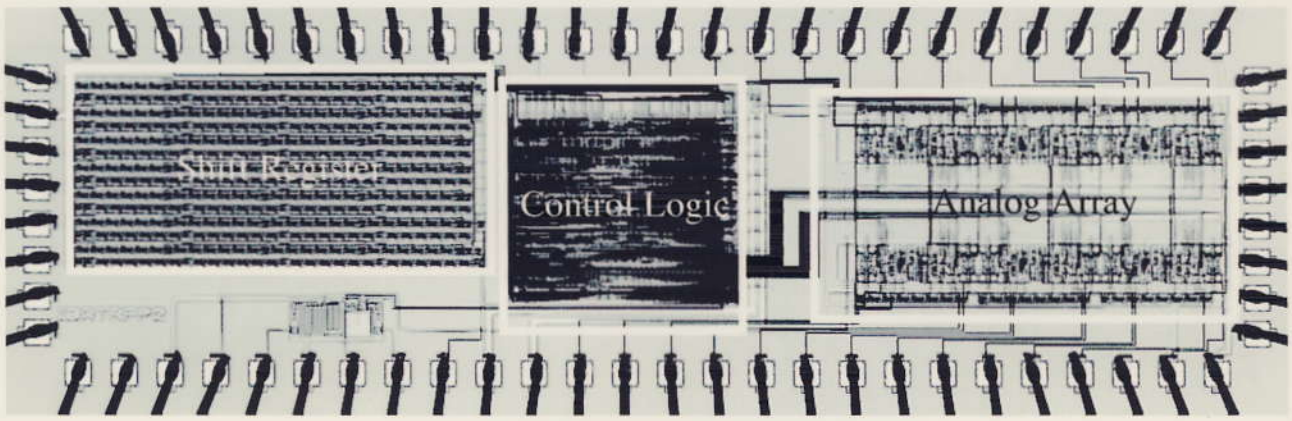


Figure 3: Die photo of FPAA Prototype

60 MHz, 2000 V/μs Monolithic Op Amp

AD844

FEATURES

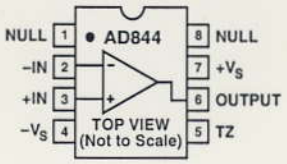
Wide Bandwidth: 60 MHz at Gain of –1
Wide Bandwidth: 33 MHz at Gain of –10
Very High Output Slew Rate: Up to 2000 V/μs
20 MHz Full Power Bandwidth, 20 V p-p, R_L = 500 Ω
Fast Settling: 100 ns to 0.1% (10 V Step)
Differential Gain Error: 0.03% at 4.4 MHz
Differential Phase Error: 0.158 at 4.4 MHz
Low Offset Voltage: 150 mV Max (B Grade)
Low Quiescent Current: 6.5 mA
Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS

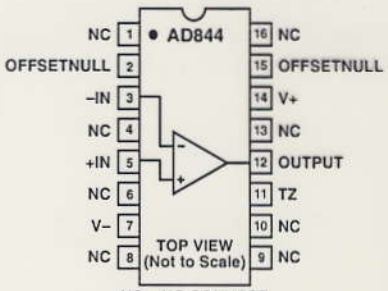
Flash ADC Input Amplifiers
High Speed Current DAC Interfaces
Video Buffers and Cable Drivers
Pulse Amplifiers

CONNECTION DIAGRAMS

8-Lead PDIP (N) and CERDIP (Q) Packages



16-Lead SOIC (R) Package



NC = NO CONNECT

GENERAL DESCRIPTION

The AD844 is a high speed monolithic operational amplifier fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. It combines high bandwidth and very fast large signal response with excellent dc performance. Although optimized for use in current-to-voltage applications and as an inverting mode amplifier, it is also suitable for use in many noninverting applications.

The AD844 can be used in place of traditional op amps, but its current feedback architecture results in much better ac performance, high linearity, and an exceptionally clean pulse response.

This type of op amp provides a closed-loop bandwidth that is determined primarily by the feedback resistor and is almost independent of the closed-loop gain. The AD844 is free from the slew rate limitations inherent in traditional op amps and other current-feedback op amps. Peak output rate of change can be over 2000 V/μs for a full 20 V output step. Settling time is typically 100 ns to 0.1%, and essentially independent of gain. The AD844 can drive 50 Ω loads to ±2.5 V with low distortion and is short circuit protected to 80 mA.

The AD844 is available in four performance grades and three package options. In the 16-lead SOIC (R) package, the AD844J is specified for the commercial temperature range of 0°C to 70°C. The AD844A and AD844B are specified for the industrial temperature range of –40°C to +85°C and are available in the CERDIP (Q) package. The AD844A is also available in an 8-lead PDIP (N). The AD844S is specified over the military temperature range of –55°C to +125°C. It is available in the 8-lead CERDIP (Q) package. A and S grade chips and devices processed to MIL-STD-883B, REV. C are also available.

PRODUCT HIGHLIGHTS

1. The AD844 is a versatile, low cost component providing an excellent combination of ac and dc performance.
2. It is essentially free from slew rate limitations. Rise and fall times are essentially independent of output level.
3. The AD844 can be operated from ±4.5 V to ±18 V power supplies and is capable of driving loads down to 50 Ω, as well as driving very large capacitive loads using an external network.
4. The offset voltage and input bias currents of the AD844 are laser trimmed to minimize dc errors; V_{OS} drift is typically 1 μV/°C and bias current drift is typically 9 nA/°C.
5. The AD844 exhibits excellent differential gain and differential phase characteristics, making it suitable for a variety of video applications with bandwidths up to 60 MHz.
6. The AD844 combines low distortion, low noise, and low drift with wide bandwidth, making it outstanding as an input amplifier for flash A/D converters.

REV. E

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

Table I.

Gain	R1	R2	BW (MHz)	GBW (MHz)
−1	1 kΩ	1 kΩ	35	35
−1	500 Ω	500 Ω	60	60
−2	2 kΩ	1 kΩ	15	30
−2	1 kΩ	500 Ω	30	60
−5	5 kΩ	1 kΩ	5.2	26
−5	500 Ω	100 Ω	49	245
−10	1 kΩ	100 Ω	23	230
−10	500 Ω	50 Ω	33	330
−20	1 kΩ	50 Ω	21	420
−100	5 kΩ	50 Ω	3.2	320
+100	5 kΩ	50 Ω	9	900

Response as an I-V Converter

The AD844 works well as the active element in an operational current-to-voltage converter, used in conjunction with an external scaling resistor, R1, in Figure 3. This analysis includes the stray capacitance, C_S, of the current source, which might be a high speed DAC. Using a conventional op amp, this capacitance forms a "nuisance pole" with R1 that destabilizes the closed-loop response of the system. Most op amps are internally compensated for the fastest response at unity gain, so the pole due to R1 and C_S reduces the already narrow phase margin of the system. For example, if R1 were 2.5 kΩ, a C_S of 15 pF would place this pole at a frequency of about 4 MHz, well within the response range of even a medium speed operational amplifier. In a current feedback amp, this nuisance pole is no longer determined by R1 but by the input resistance, R_{IN}. Since this is about 50 Ω for the AD844, the same 15 pF forms a pole at 212 MHz and causes little trouble. It can be shown that the response of this system is:

$$V_{OUT} = -I_{sig}\frac{K\,R1}{(1+s_{Td})(1+s_{Tn})}$$

where K is a factor very close to unity and represents the finite dc gain of the amplifier, Td is the dominant pole, and Tn is the nuisance pole:

$$K = \frac{R_t}{R_t + R1}$$

$$Td = KR1C_t$$

$$Tn = R_{IN}C_S \quad (assuming\ R_{IN} << R1)$$

Using typical values of $R1$ = 1 kΩ and R_t = 3 MΩ, K is 0.9997; in other words, the "gain error" is only 0.03%. This is much less than the scaling error of virtually all DACs and can be absorbed, if necessary, by the trim needed in a precise system.

In the AD844, R_t is fairly stable with temperature and supply voltages, and consequently the effect of finite "gain" is negligible unless high value feedback resistors are used. Since that would result in slower response times than are possible, the relatively low value of R_t in the AD844 will rarely be a significant source of error.

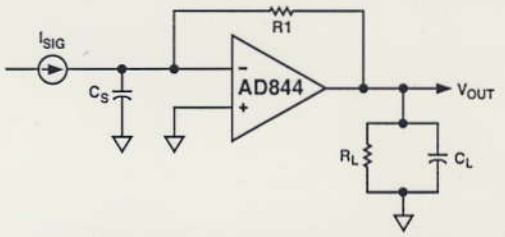


Figure 3. Current-to-Voltage Converter

Circuit Description of the AD844

A simplified schematic is shown in Figure 4. The AD844 differs from a conventional op amp in that the signal inputs have radically different impedance. The noninverting input (Pin 3) presents the usual high impedance. The voltage on this input is transferred to the inverting input (Pin 2) with a low offset voltage, ensured by the close matching of like polarity transistors operating under essentially identical bias conditions. Laser trimming nulls the residual offset voltage, down to a few tens of microvolts. The inverting input is the common emitter node of a complementary pair of grounded base stages and behaves as a current summing node. In an ideal current feedback op amp, the input resistance would be zero. In the AD844, it is about 50 Ω.

A current applied to the inverting input is transferred to a complementary pair of unity-gain current mirrors that deliver the same current to an internal node (Pin 5) at which the full output voltage is generated. The unity-gain complementary voltage follower then buffers this voltage and provides the load driving power. This buffer is designed to drive low impedance loads, such as terminated cables, and can deliver ±50 mA into a 50 Ω load while maintaining low distortion, even when operating at supply voltages of only ±6 V. Current limiting (not shown) ensures safe operation under short circuited conditions.

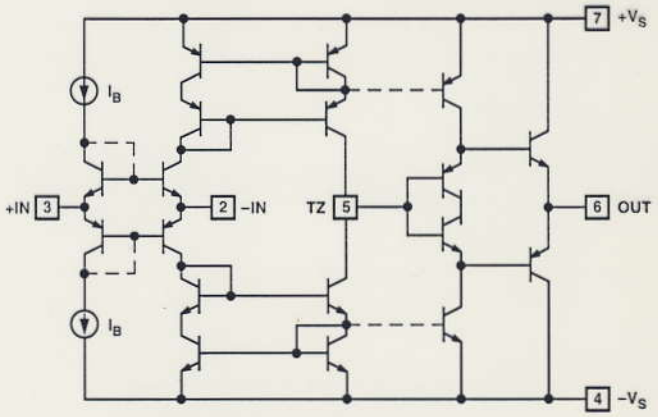


Figure 4. Simplified Schematic

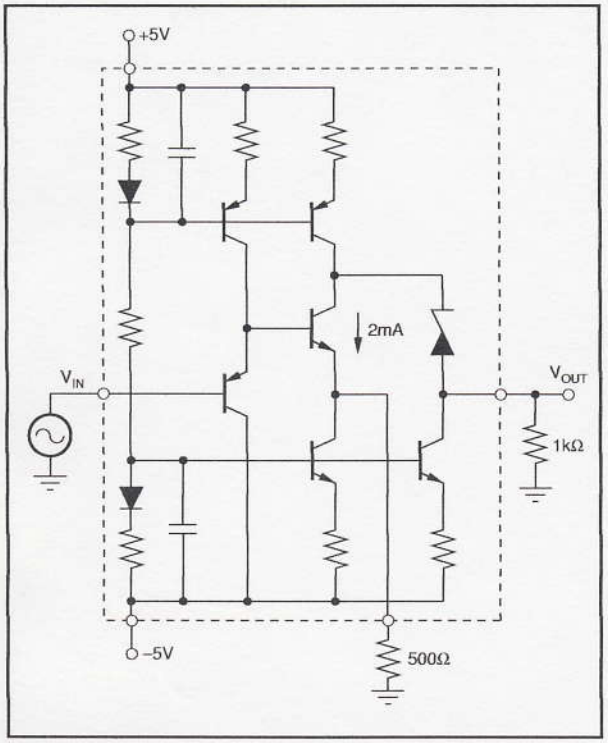


FIGURE 3. Circuit with Constant Current Sources.

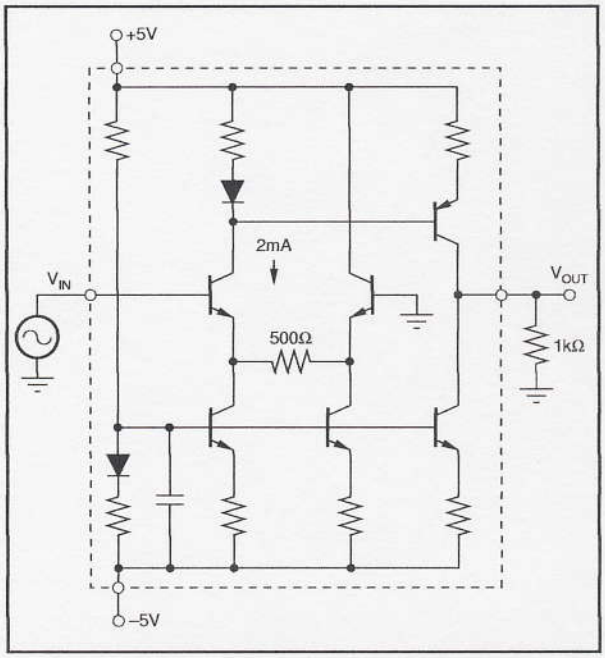


FIGURE 5. Differential Amplifier for Compensation of V_{IO}.

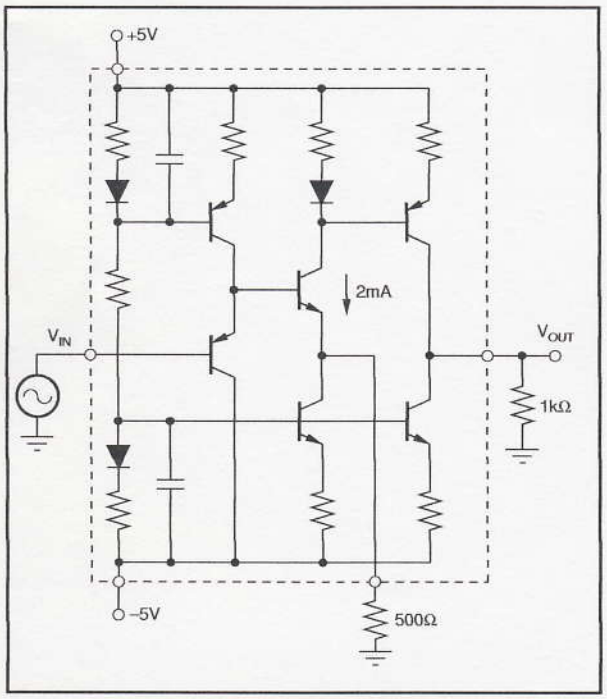


FIGURE 4. Insertion of PNP Current Mirror.

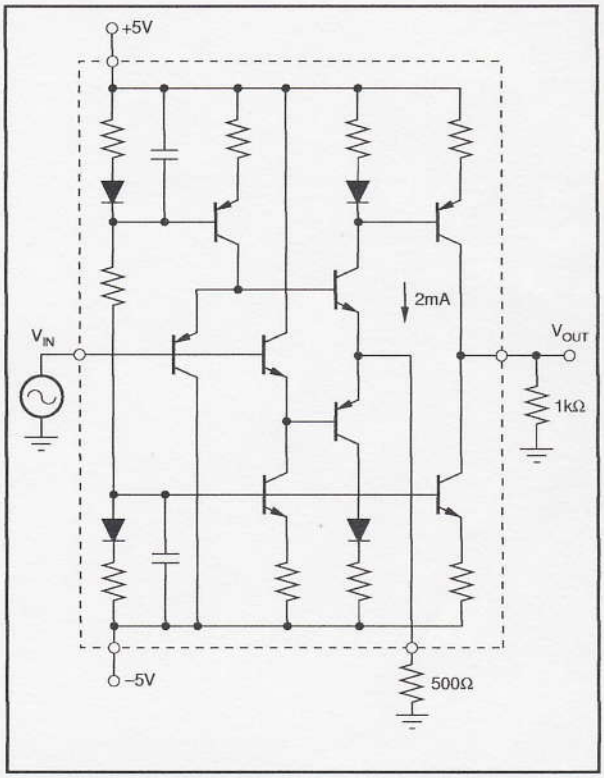


FIGURE 6. Diamond Structure.

Figure 4 shows a variation comparable to Figure 3, in which the V_{OO} is avoided using a current mirror instead of a zener diode. Figure 5 shows how a differential amplifier can be used to compensate the V_{IO} in place of the previously inserted complementary emitter follower. This method has the disadvantage that the emitter resistor (500Ω) is connected on both sides to "hot" adaptors. The previously discussed methods using zener diodes or resistors instead of current sources are also possible here. Figure 6 illustrates the most developed and elegant method with a complementary