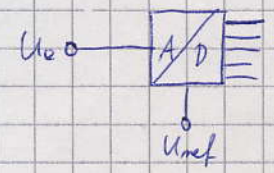
7.6.05

A/D - Wandler

Prinzip



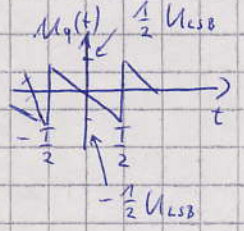
$$Z = \text{Round}\left(U_e \cdot \frac{2^N}{U_{ref}}\right)$$

Folie

a) ~~Quantis~~ Wertdiskretisierung

Quantisierungsfehler U_q wird als Rauschen modelliert → Quantisierungsrauschen

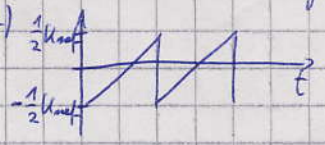
zeitlich linear ansteigendes Signal



Effektivwert: $U_q = \sqrt{\frac{1}{T}\int_{-\frac{T}{2}}^{T/2} u_q^2(t)\,dt}$

$$= \sqrt{\frac{1}{T}\int_{-\frac{T}{2}}^{T/2}\left(-U_{LSB}\cdot\frac{t}{T}\right)^2 dt} = \sqrt{\frac{U_{LSB}^2}{T^3}\cdot\frac{t^3}{3}\Big|_{-\frac{T}{2}}^{\frac{T}{2}}} = \underline{\underline{\frac{U_{LSB}}{\sqrt{12}}}}$$

daraus: Signal-zu-Rauschabstand bei Vollaussteuerung mit Sägezahn



$$SNR = 20\,\log\left(\frac{U_e}{U_q}\right)$$

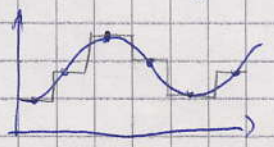
$$= 20\,\log\left(\frac{U_{ref}/\sqrt{12}}{U_{LSB}/\sqrt{12}}\right) = 20\,\log\left(\frac{U_{ref}}{U_{LSB}}\right) = 20\log\left(2^N\right)$$

$$SNR = 20\cdot N\cdot \log 2 = \underline{n\cdot 6{,}02\,dB}$$

→ Erhöhung der Auflösung um 1 Bit erhöht das SNR um 6 dB.

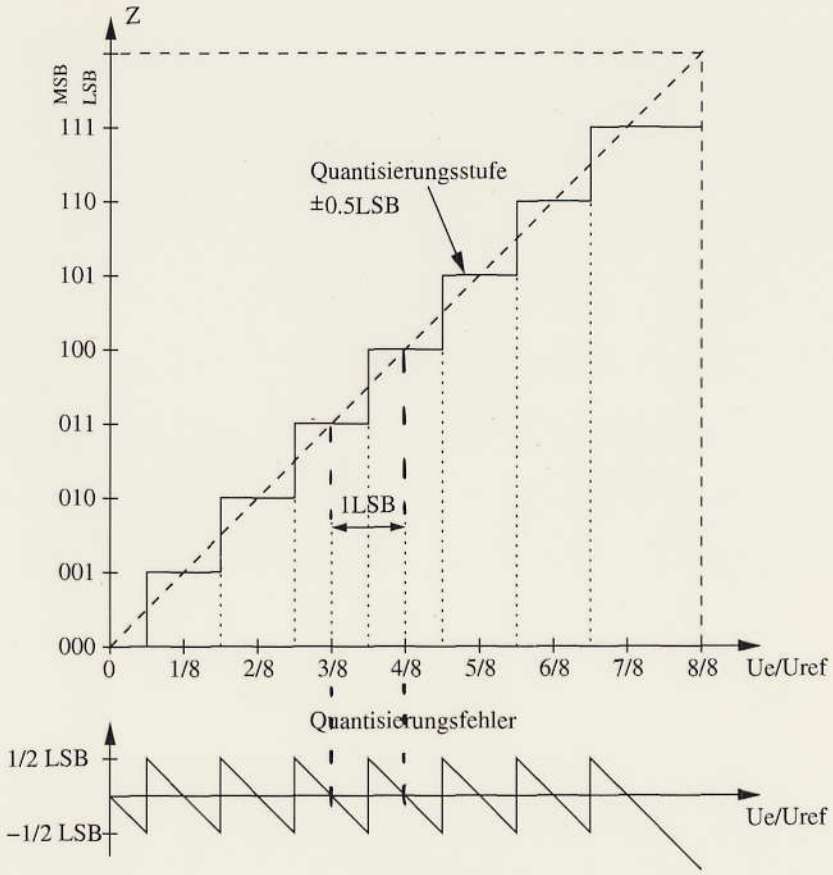
- für Sinussignal: $SNR = n\cdot 6{,}02\,dB + 1{,}76\,dB$ (bei gleichem Quantisierungsfehler-Verhalten)

b) Zeitdiskretisierung

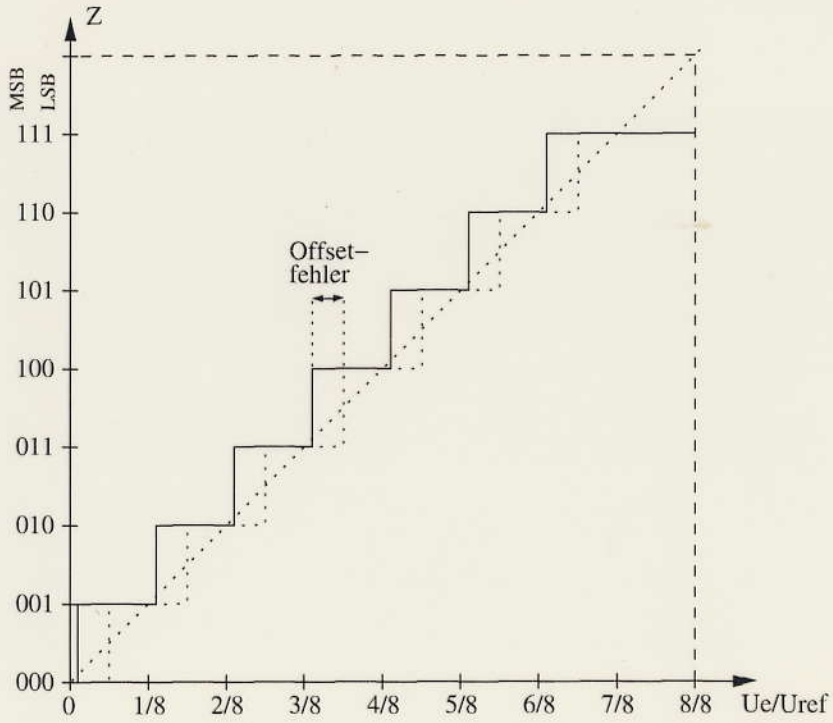


→ Abtasttheorem

Ideale Kennlinie eines 3Bit-Wandlers



Offsetfehler



Kenngrößen

Auflösung in Bit

Wandlerrate in S/s

statische Fehler

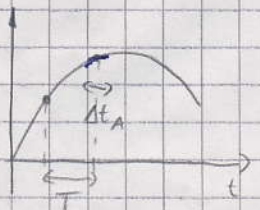
- Offsetfehler → Folie
- Verstärkungsfehler → Folie
- Nichtlinearität → Folie

} lineare Fehler

hohe differentielle NL führt bei DACs zu Monotoniefehlern, bei ADCs zu fehlenden / ausgelassenen Werten → missing codes

dynamische Fehler

Verschiebung der Abtastzeitpunkte (Jitter) → Aperturfehler



Sinus-Signal: - größter Fehler entsteht im Nulldurchgang (größter Anstieg)

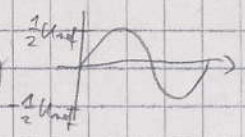
$$\left.\frac{dU}{dt}\right|_{max} = \hat{U} \cdot \omega$$

Fehler: $\Delta U = \hat{U}\, \omega_{max}\, \Delta t_A$

Genauigkeit bleibt erhalten für $\Delta U < U_{LSB}$

$$\rightarrow \Delta t_A < \frac{U_{LSB}}{\hat{U}\,\omega_{max}} = \frac{2U_{LSB}}{U_{ref}\,\omega_{max}}$$

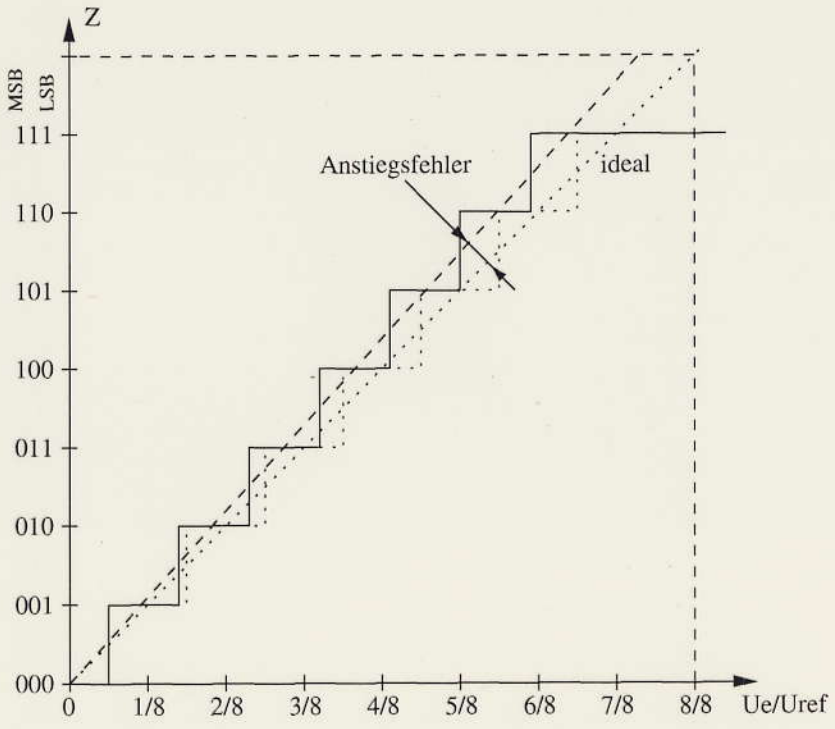
für symmetrischen Eingang



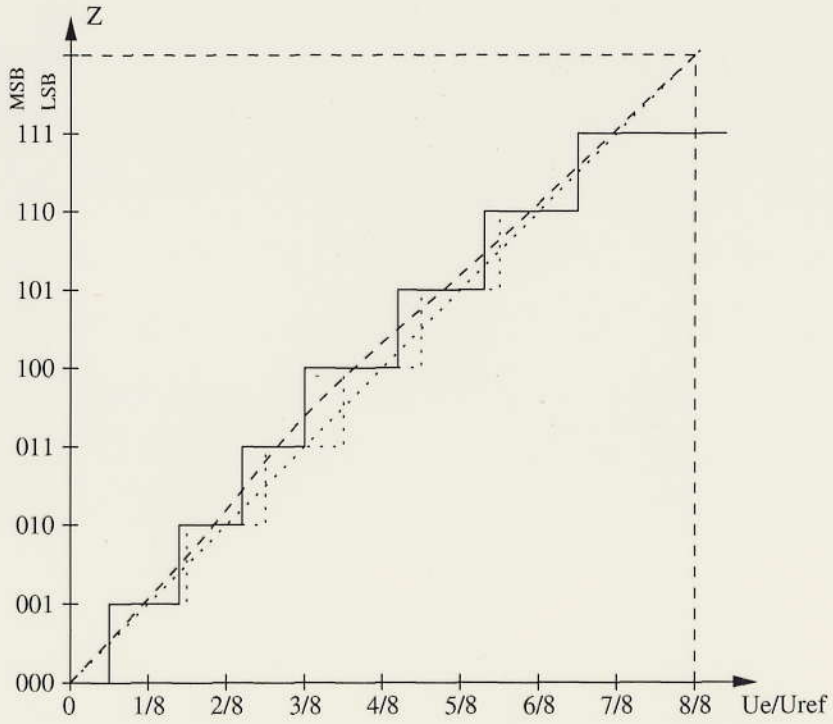
Bsp. 8 Bit A/D-Wandler $\quad \frac{2U_{LSB}}{U_{ref}} = \frac{1}{128}$, $f_{max} = 10\,MHz$

$$\rightarrow \Delta t_A < 250\,ps$$

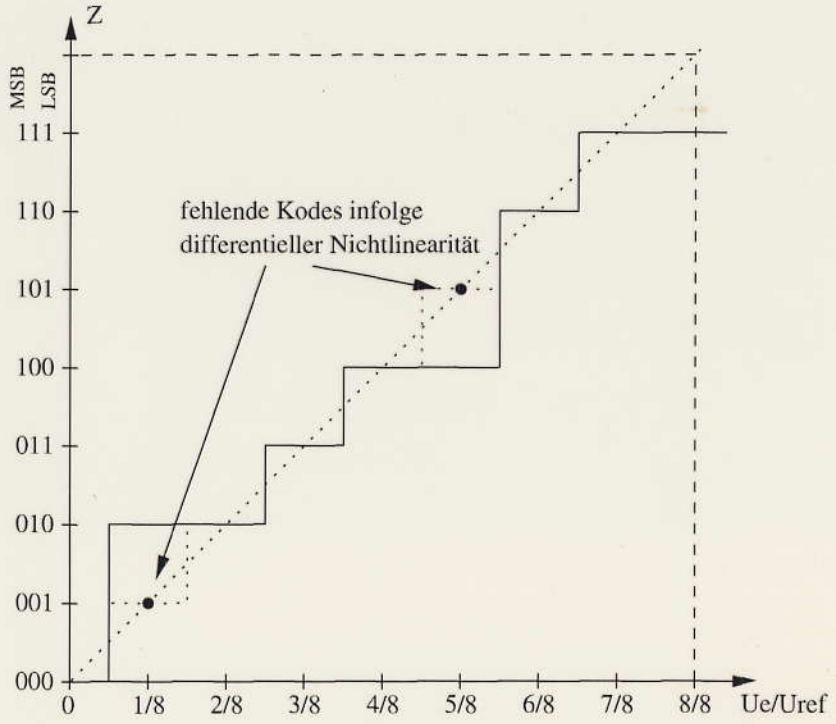
Verstärkungsfehler



Integrale Nichtlinearität



Differentielle Nichtlinearität

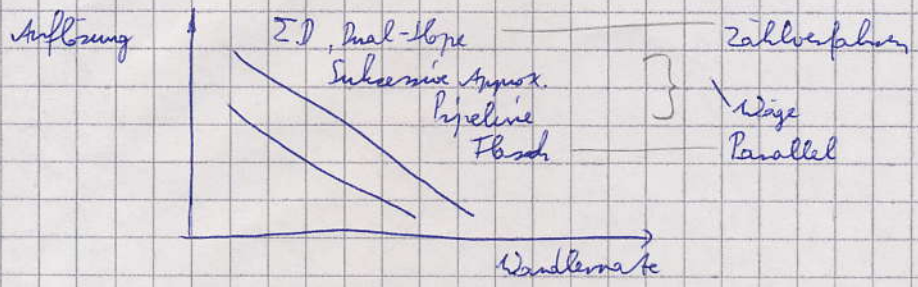


Realisierungen

Prinzipieller Aufbau

S&H Stufe bereits im ADC enthalten

Wandlertypen



a) **Flash-Wandler** Folie

Komplement zum Parallel-DAC

- 2^n Komparatoren nötig
- Einsatz bei niedrigen Auflösungen $N \leq 8$ Bit
- Sehr hohe Wandlerraten bis zu einigen GS/s Folie MAX 104

b) **Sukzessive Approximation Wandler**

Folie

Komparatorvariante:
- N Takte zur Wandlung in N Bit nötig
- statt Komparator auch ADC mit >1 Bit Auflösung verwendbar, Verringerung der Taktanzahl
- DAC muß volle N Bit Genauigkeit besitzen

- Folie MAX 146

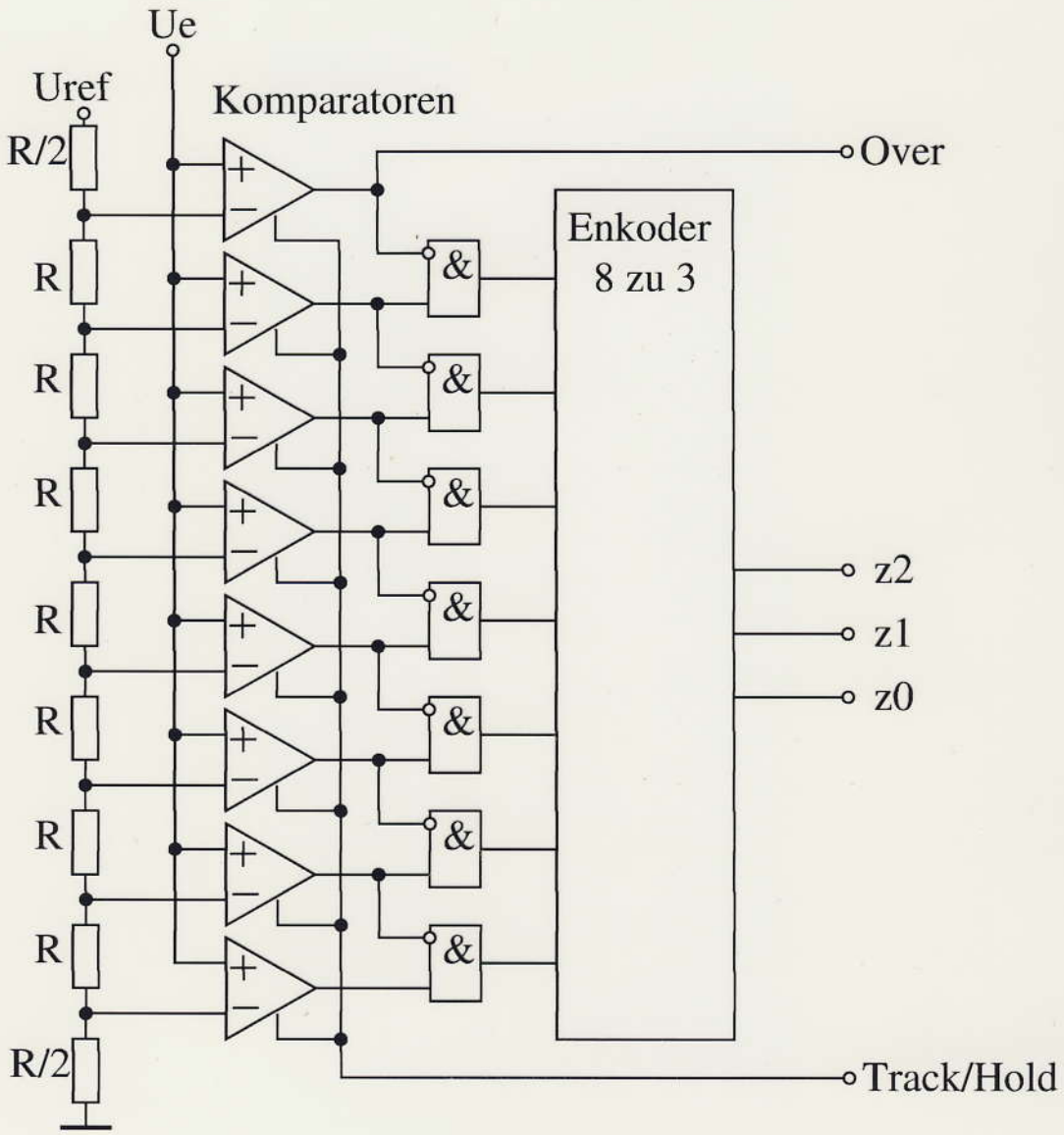
c) **Pipeline-Wandler**

Prinzip Folie
- ADC gibt n Bit aus
- DAC wandelt die n Bit zurück
- Differenzbildung
- Verstärkung der Differenz mit 2^n

- Datenausgabe erfolgt zu jedem Takt
- Latenzzeit (Zeit zwischen Anlegen Ue und Ausgabe Daten) = T · Stufenanzahl

- DAC, Differenzbildung und Verstärkung brauchen volle Genauigkeit
- ADC braucht nicht volle Genauigkeit bei Ausgabe von n+x Bit (digitale Fehlerkorrektur)

Parallelwandler



±5V, 1Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier

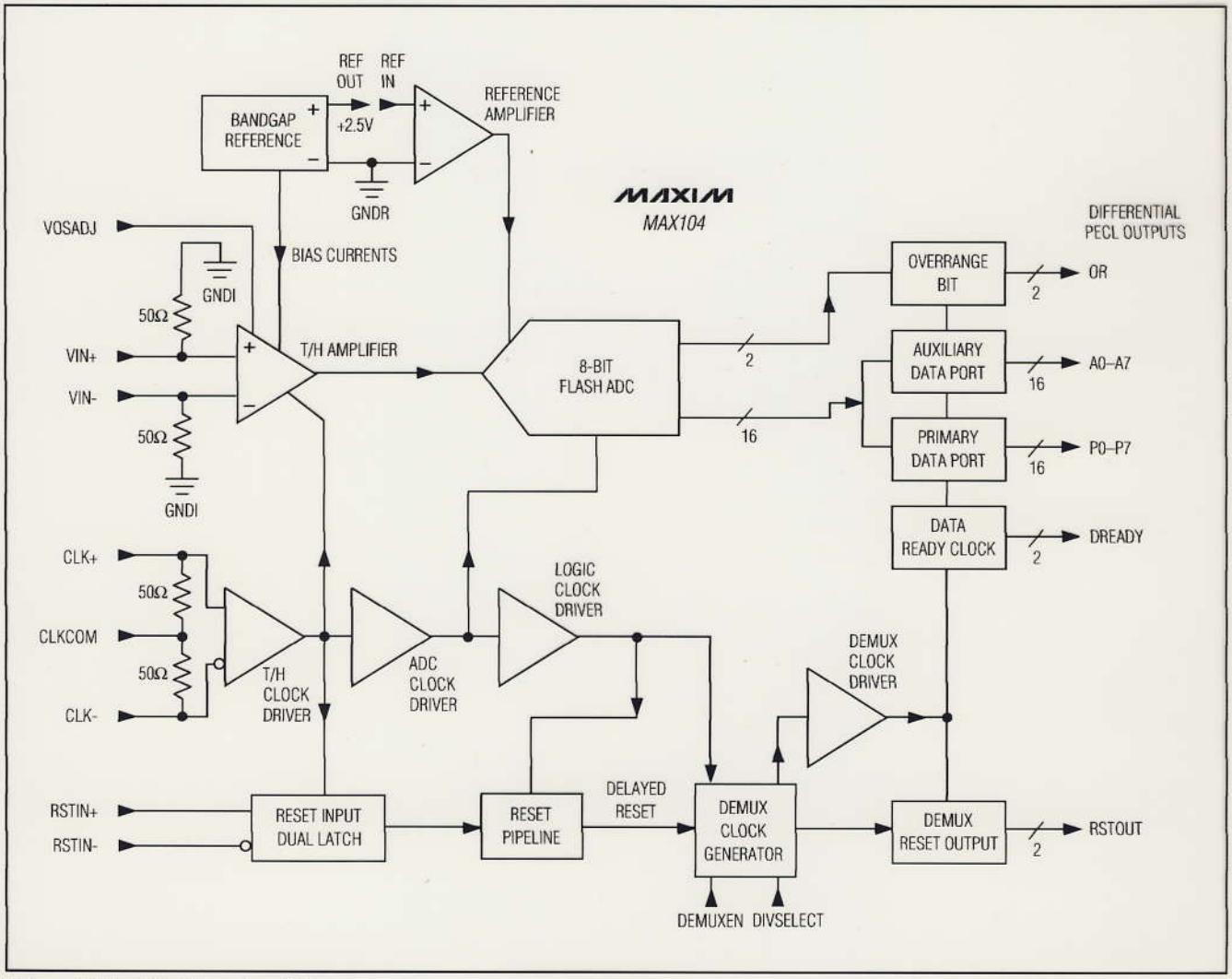


Figure 1. Simplified Functional Diagram

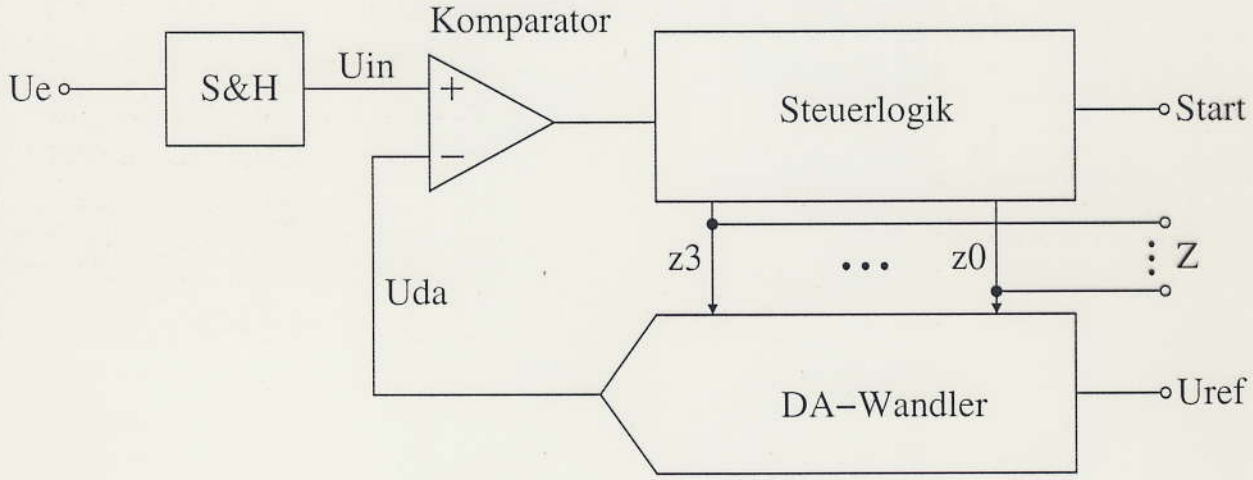
Detailed Description

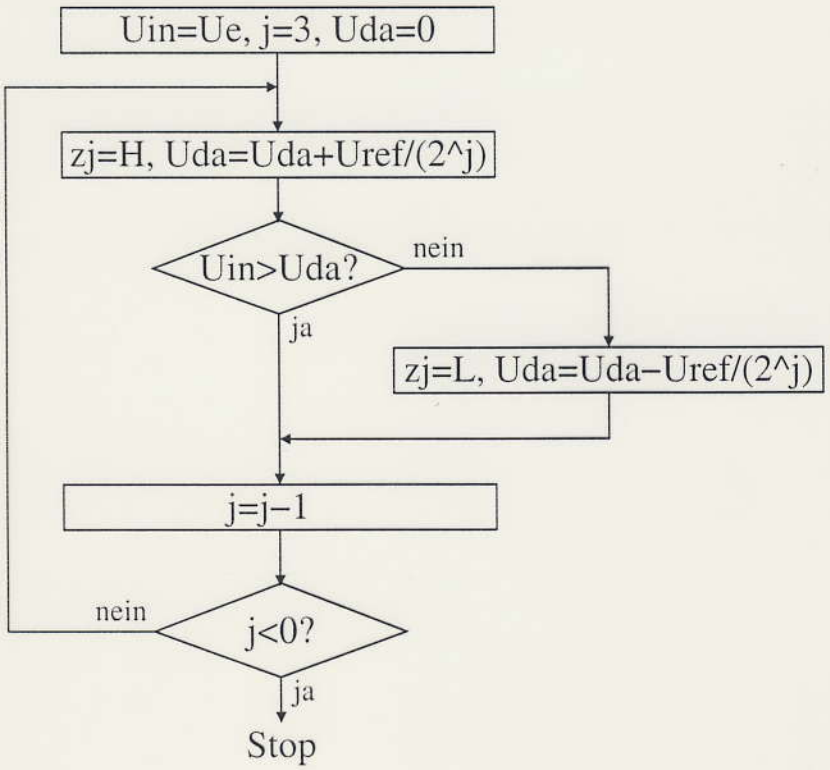
The MAX104 is an 8-bit, 1Gsps flash analog-to-digital converter (ADC) with on-chip track/hold (T/H) amplifier and differential PECL-compatible outputs. The ADC (Figure 1) employs a fully differential 8-bit quantizer and a unique encoding scheme to limit metastable states to typically one error per 10^{16} clock cycles, with no error exceeding 1LSB max.

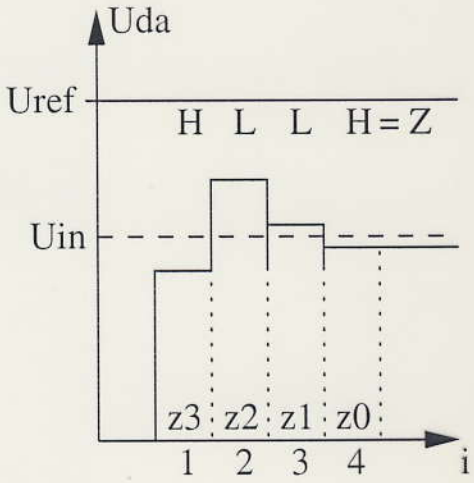
An integrated 8:16 output demultiplexer simplifies interfacing to the part by reducing the output data rate to one-half the sampling clock rate. This demultiplexer has internal reset capability that allows multiple MAX104s to be time-interleaved to achieve higher effective sampling rates.

When clocked at 1Gsps, the MAX104 provides a typical effective number of bits (ENOB) of >7.5 bits at an analog input frequency of 500MHz. The analog input of the MAX104 is designed for differential or single-ended use with a ±250mV full-scale input range. In addition, this ADC features an on-chip +2.5V precision bandgap reference. If desired, an external reference can also be used.

Wandler mit sukzessiver Approximation







Detailed Description

The MAX146/MAX147 analog-to-digital converters (ADCs) use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). Figure 3 is a block diagram of the MAX146/MAX147.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the equivalent input circuit (Figure 4). In single-ended mode, IN+ is internally switched to CH0–CH7, and IN- is switched to COM. In differential mode, IN+ and IN- are selected from the following pairs: CH0/CH1, CH2/CH3, CH4/CH5, and CH6/CH7. Configure the channels with Tables 2 and 3.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. To accomplish this, connect a 0.1µF capacitor from IN- (the selected analog input) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply COM. This unbalances node ZERO at the comparator's input. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 12-bit resolution. This action is equivalent to transferring a 16pF x [(V_{IN+}) - (V_{IN-})] charge from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to COM, and the converter samples the "+" input. If the converter is set up for differential inputs, IN- connects to the "-" input, and the difference of |IN+ - IN-| is sampled. At the end of the conversion, the positive input connects back to IN+, and C_{HOLD} charges to the input signal.

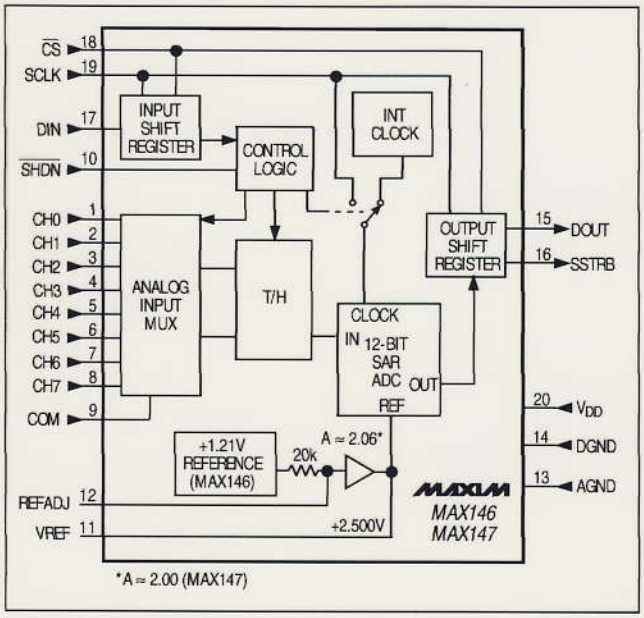


Figure 3. Block Diagram

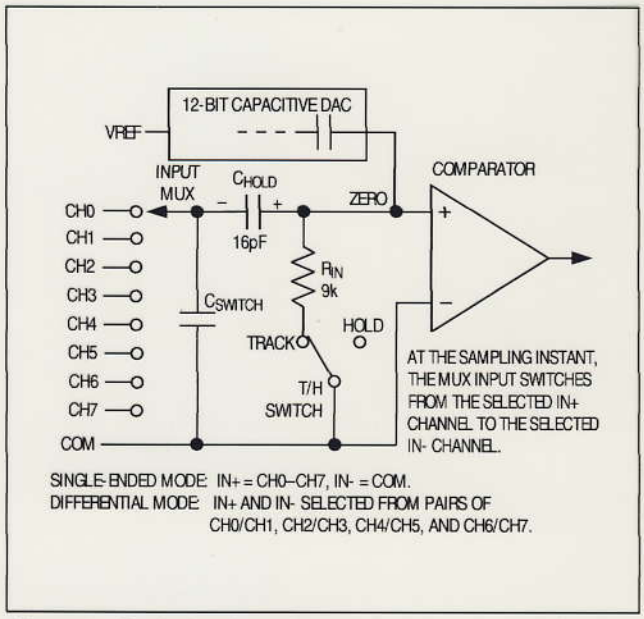
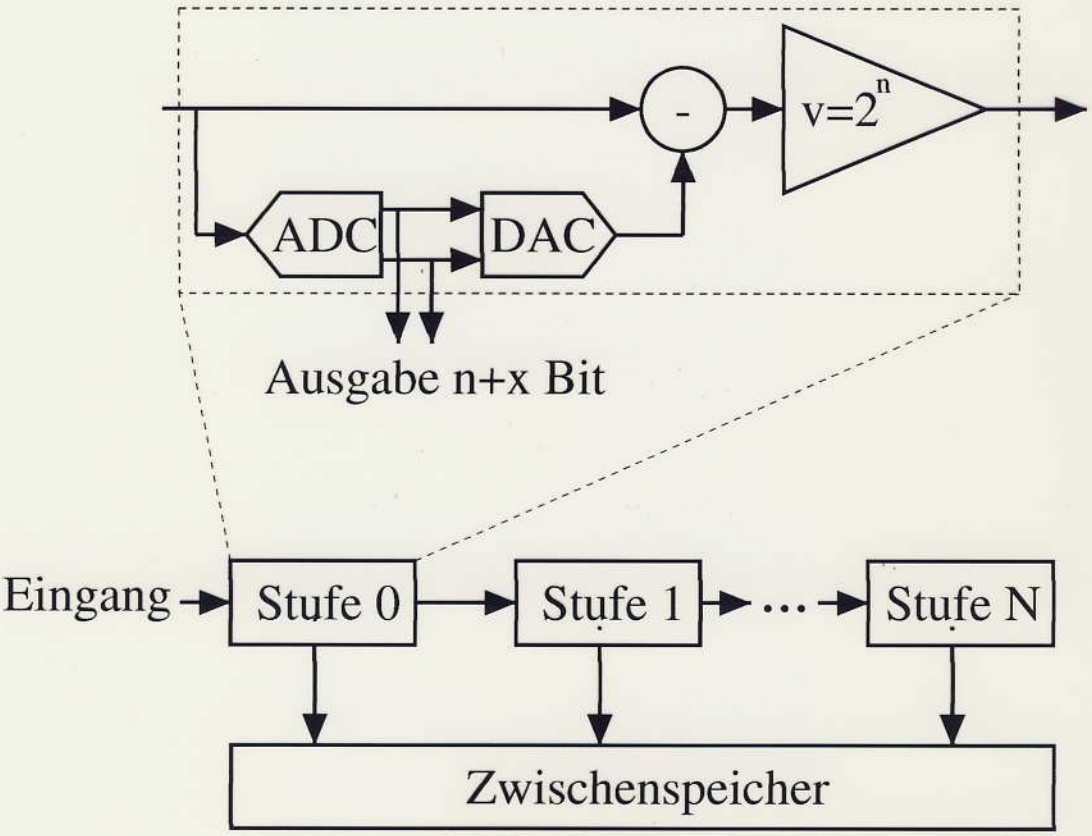


Figure 4. Equivalent Input Circuit

Pipeline AD-Wandler



+5V Single-Supply, 1Msps, 16-Bit Self-Calibrating ADC

Detailed Description

Converter Operation

The MAX1200 is a 16-bit, monolithic analog-to-digital converter (ADC) capable of conversion rates up to 1Msps. It uses a multistage, fully differential, pipelined architecture with digital error correction and self-calibration to provide typically 91dB spurious-free dynamic range at a 1Msps sampling rate. It also provides excellent SNR and THD performance up to the Nyquist frequency. This makes the device suitable for applications such as data acquisition, high-resolution imaging, scanners, digital communication, and instrumentation.

Figure 1 shows the simplified, internal structure of the ADC. A switched-capacitor, pipelined architecture is used to digitize the signal at a high throughput rate. The first four stages of the pipeline use a low-resolution quantizer to approximate the input signal. The multiplying digital-to-analog converter (MDAC) stage is used to subtract the quantized analog signal from the input. The residue is then amplified with a fixed gain and passed on to the next stage. The accuracy of the converter is improved by a digital calibration algorithm which corrects for mismatches between the capacitors in the switched-capacitor MDAC. Note that the pipeline introduces latency of four sampling periods between the input being sampled and the output appearing at D15–D0.

While the device can handle both single-ended or differential inputs (see the *Requirements for Reference and Analog Signal Inputs* section), the latter mode of operation will guarantee best THD and SFDR performance. The differential input provides the following advantages compared to a single-ended operation:

- Twice as much signal input span
- Common-mode noise immunity
- Virtual elimination of the even-order harmonics
- Less stringent requirements on the input signal processing amplifiers

Requirements for Reference and Analog Signal Inputs

Fully differential switched-capacitor circuits (SC) are used for both the reference and analog inputs (Figure 2). This allows either single-ended or differential signals to be used in the reference and/or analog signal paths. The signal voltage on these pins (INP, INN, RFP_, RFN_) should never exceed the analog supply rail, AV_{DD}, nor fall below ground.

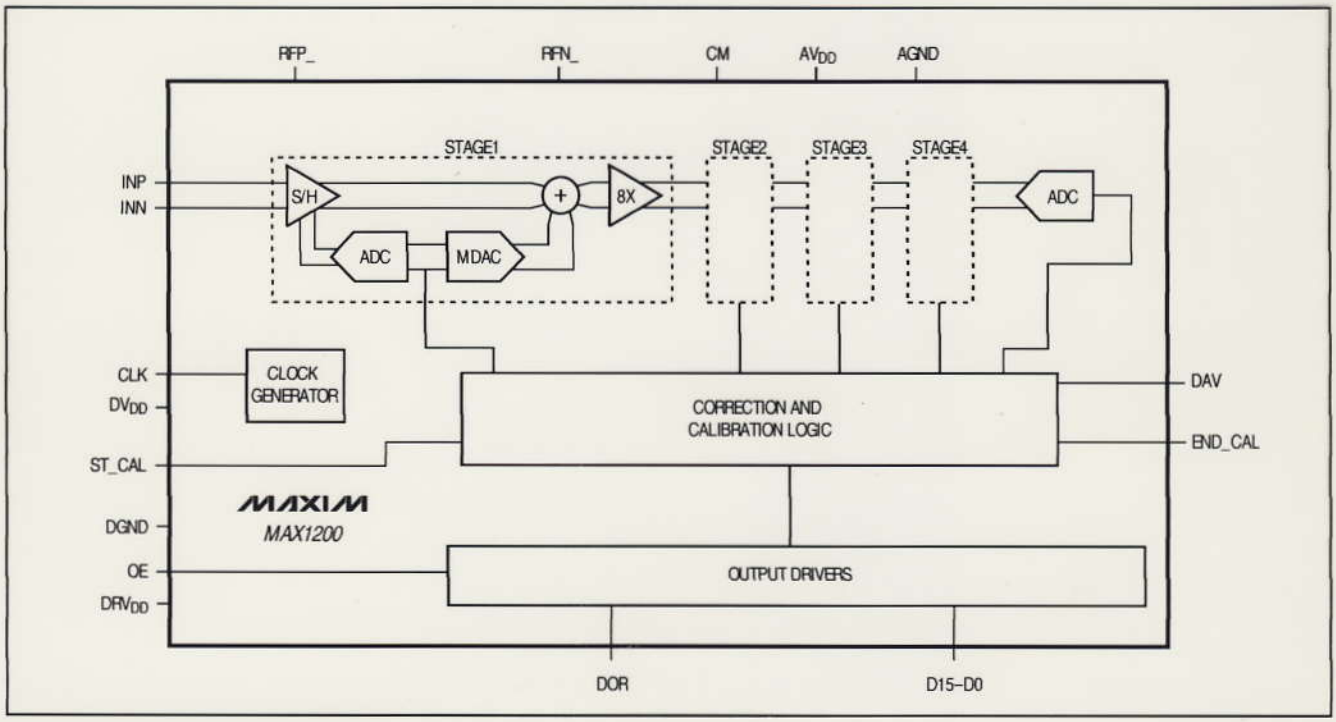


Figure 1. Internal Functional Diagram

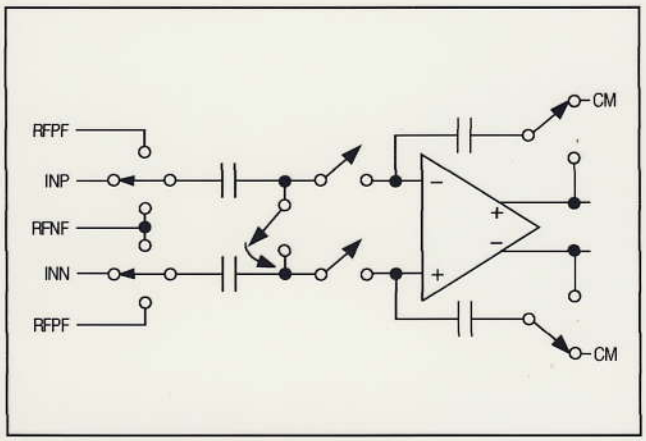


Figure 2. Simplified MDAC Architecture

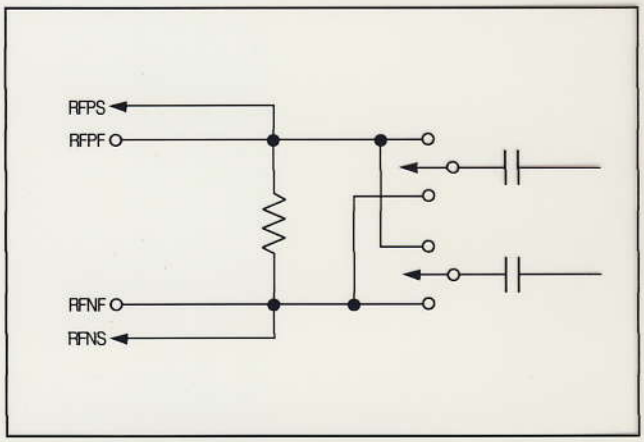


Figure 3. Equivalent Input at the Reference Pins. The sense pins should not draw any DC current.

Choice of Reference

It is important to choose a low-noise reference such as the MAX6341, which can provide both excellent load regulation and low temperature drift. The equivalent input circuit for the reference pins is shown in Figure 3. Note that the reference pins drive approximately 1kΩ of resistance on-chip. They also drive a switched capacitor of 21pF. To meet the dynamic performance, the reference voltage is required to settle to 0.0015% within one clock cycle. Carefully choose an appropriate driving circuit (Figure 4). The capacitors at the reference pins (RFPF, RFNF) provide the dynamic charge required during each clock cycle, while the op amps ensure accuracy of the reference signals. These capacitors must have low dielectric-absorption characteristics, such as polystyrene or teflon capacitors.

The reference pins can be connected to either single-ended or differential voltages within the specified maximum levels. Typically the positive reference pin (RFPF) would be driven to +4.096V, and the negative reference pin (RFNF) connected to analog ground for best SNR performance. If THD performance is more important to the application than signal-to-noise ratio, choose a lower level, differential voltage such as V_{RFPS} = +3.5V and V_{RFNS} = +1.5V.

There are sense pins, RFPS and RFNS, which can be used with external amplifiers to compensate for any resistive drop on these lines, internal or external to the chip. Ensure a correct reference voltage by using proper Kelvin connections at the sense pins.

Common-Mode Voltage

The switched-capacitor input circuit at the analog input allows signals between AGND and the analog power supply. Since the common-mode voltage has a strong influence on the performance of the ADC, the best results are obtained by choosing V_{CM} = (V_{RFPS} + V_{RFNS}) / 2. This can be achieved by using a resistive divider between the two reference potentials. Figure 4 shows a typical driving circuit for good dynamic performance.

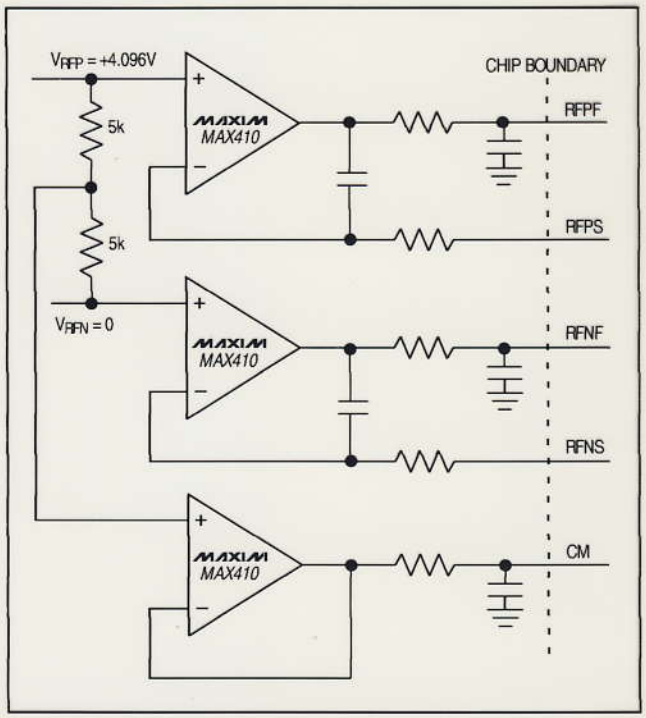


Figure 4. Drive Circuit for Reference Pins and Common-Mode Pin

d) Sigma - Delta - Wandler

Folie, Schaltung

Analyse der Signale:

Integrator: $b(k) = b(k-1) + a(k) \cdot T$

Komparator: $y'(k) = \text{sign}(b(k)) = \begin{cases} -1 & b(k) < 0 \\ 1 & b(k) > 0 \end{cases}$

~~D/A Wandler:~~

Totzeitglied: $y(k) = y'(k-1)$

D/A - Wandler: $c(k) = y(k) \cdot x_{ref}$

Summationsknoten: $a(k) = x(k) - y(k) \cdot x_{ref}$

$\rightsquigarrow b(k) = b(k-1) + T \cdot (x(k) - \text{sign}(b(k-1)))$ Zustandsgleichung

$y(k) = \text{sign}(b(k-1))$ Ausgabefunktion

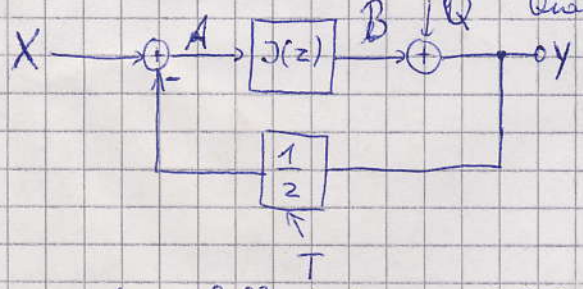
~~stabile Zustände~~: Fixpunkte:

$b(k) - b(k-1) = 0 \rightarrow x(k) - \text{sign}(b(k-1)) = 0$

$x_1 = -1 \quad x_2 = 1$

im Intervall $[-1, 1]$ ~~Arctan~~ existieren unendlich viele instabile Zustände

- lineare Analyse als zeitdiskretes System



Quantisierungsweißes Spektrum

- DAC wird als $V = 1$ - Übertrag modelliert

Korrespondenztabelle: Integrator, $D(z) = \frac{1}{1-z^{-1}}$

Signalübertragungsfunktion

$Q = 0$, $Y(X)$

$A = -\frac{Y}{z} + X$

$Y = A(1-z^{-1})$

$Y(1-z^{-1}+z^{-1}) = X$

$Y = X$

Störübertragungsfunktion

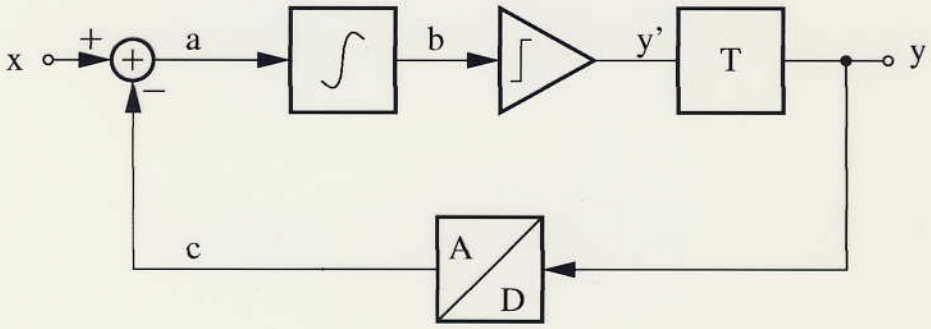
$X = 0$, $Y(Q)$

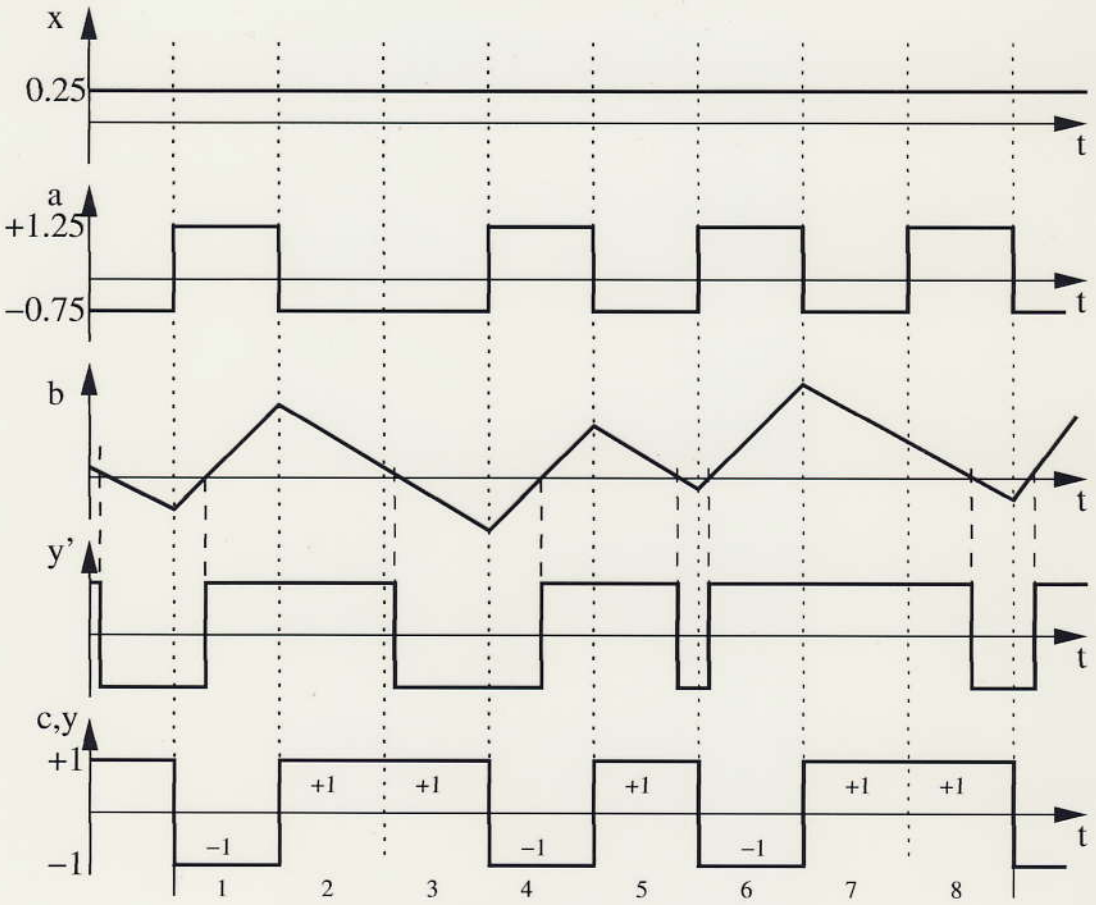
$A = -\frac{Y}{z}$

$Y = Q + \frac{A}{1-z^{-1}}$

$Y = Q(1-z^{-1})$

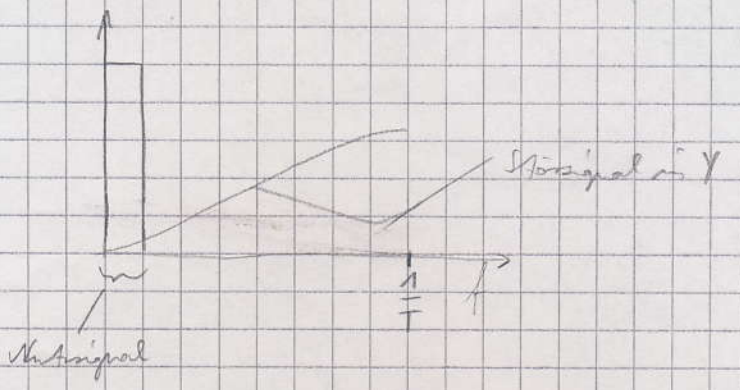
Sigma-Delta-Wandler 1. Ordnung





$$[\ 5*(+1) + 3*(-1)\ ]/8 = 0.25$$

Spektrum



- Ziel: Minimierung des Störanteils in Y

→ Filterung. einfache Variante: Mittelwertbildung über N Takte, liefert sinc (x) im Frequenzbereich
→ Folie unten

- Architekturerweiterungen:
  - mehrwertige Komparatoren
  - mehrere Integratoren → Modulatoren höherer Ordnung
  - aufwendigere Dekodieralgorithmen
- Vorteil: - sehr einfache Architektur
  - einfache Dekodierung über Mittelwertbildung möglich
  - bei konstantem Eingangssignal ist die Auflösung über die Sequenzlänge „einstellbar"
- Nachteil: - hohe Überabtastung notwendig (bei erster Ordnung 2^N Takte für N Bit)

→ niedrige Wandlungsraten, hohe Auflösungen

16-Bit 900 kSPS Σ-Δ ADC with a Programmable Postprocessor

AD7725

FEATURES

Programmable Filtering:
- Any Characteristic up to 108 Tap FIR and/or IIR

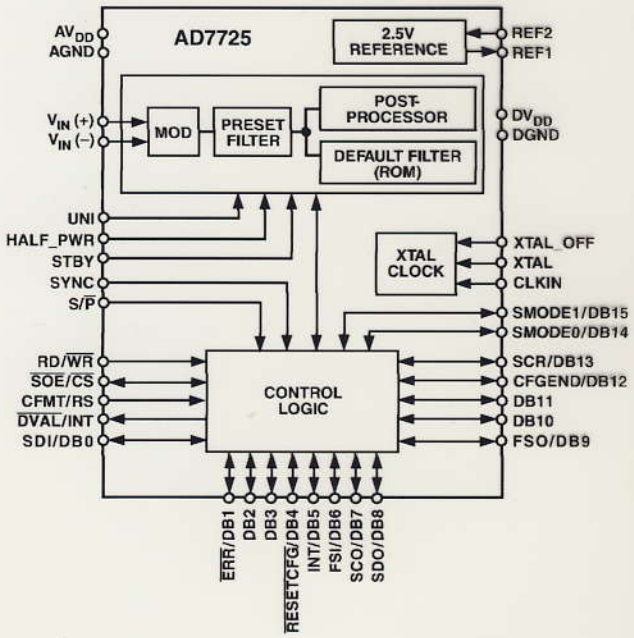
Polynomial Signal Conditioning up to 8th Order
Programmable Decimation and Output Word Rate
Flexible Programming Modes:
- Boot from DSP or External EPROM
- Parallel/Serial Interface

Internal Default Filter for Evaluation
14.4 MHz Max Master Clock Frequency
0 V to +4 V (Single-Ended) or ±2 V (Differential) Input Range
Power Supplies: AV_{DD}, DV_{DD}: 5 V ± 5%
On-Chip 2.5 V Voltage Reference
44-Lead MQFP Package

TYPICAL APPLICATIONS

Radar
Sonar
Auxiliary Car Functions
Medical Communications

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7725 is a complete 16-bit, Σ-Δ analog-to-digital converter with on-chip, user-programmable signal conditioning. The output of the modulator is processed by three cascaded finite impulse response (FIR) filters, followed by a fully user-programmable postprocessor. The postprocessor provides processing power of up to 130 million accumulates (MAC) per second. The user has complete control over the filter response, the filter coefficients, and the decimation ratio.

The postprocessor permits the signal conditioning characteristics to be programmed through a parallel or serial interface. It is programmed by loading a user-defined filter in the form of a configuration file. This filter can be loaded from a DSP or an external serial EPROM. It is generated using a digital filter design package called Filter Wizard, which is available from the AD7725 section on the Analog Devices website.

Filter Wizard allows the user to design different filter types and generates the appropriate configuration file to be downloaded to the postprocessor. The AD7725 also has an internal default filter for evaluation purposes.

It provides 16-bit performance for input bandwidths up to 350 kHz with an output word rate of 900 kHz maximum. The input sample rate is set either by the crystal oscillator or an external clock.

This part has an accurate on-chip 2.5 V reference for the modulator. A reference input/output function allows either the internal reference or an external system reference to be used as the reference source for the modulator.

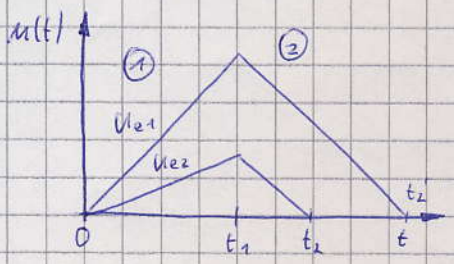
The device is available in a 44-lead MQFP package and is specified over a –40°C to +85°C temperature range.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

e) Dual-Slope-Wandler

Prinzip



① Aufintegrieren der Eingangsspannung über eine feste Zeit t_1, $C_1 \sim U_e$

② Abintegrieren mit $U_{ref} \rightarrow C_2 = konst.$, Messen der Zeit $t_2 - t_1 \sim U_e$

$$U(t_2) = U_e \cdot C_i \cdot t_2$$

$$t_2 - t_1 = \frac{U(t_2)}{U_{ref} \cdot C_i} = \frac{U_e \cdot t_1}{U_{ref}}$$

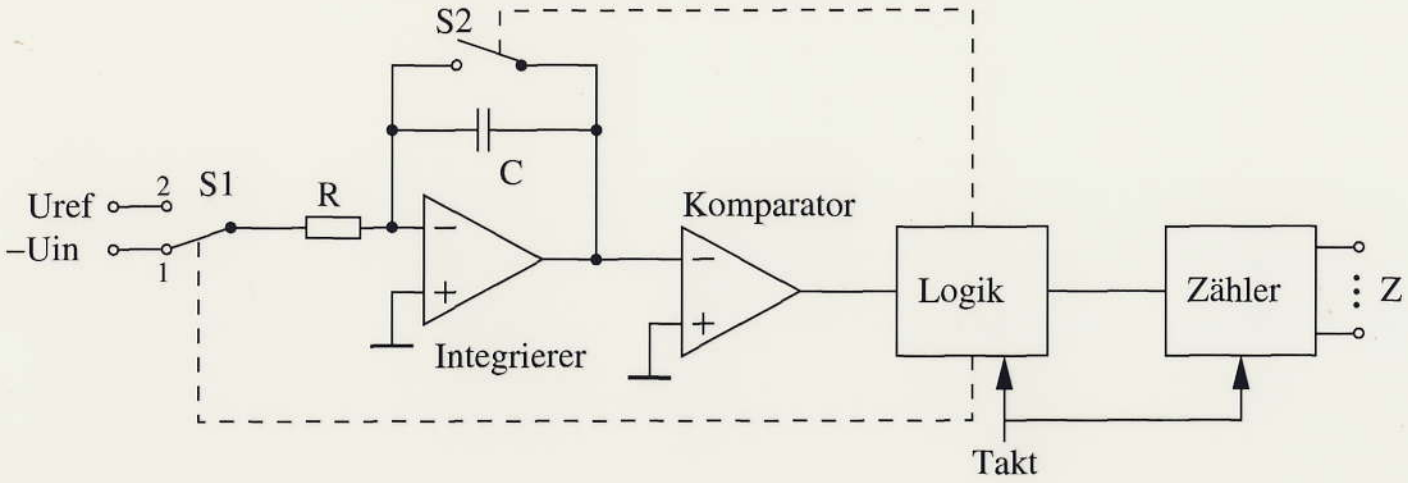
- durch Integration während t_1 wirkt der Wandler mittelwertbildend, kein S&H am Eingang nötig
- Einstellung der Integrationszeit t_1 → Störunterdrückung, z.B. Unterdrückung von Netzbrummen möglich

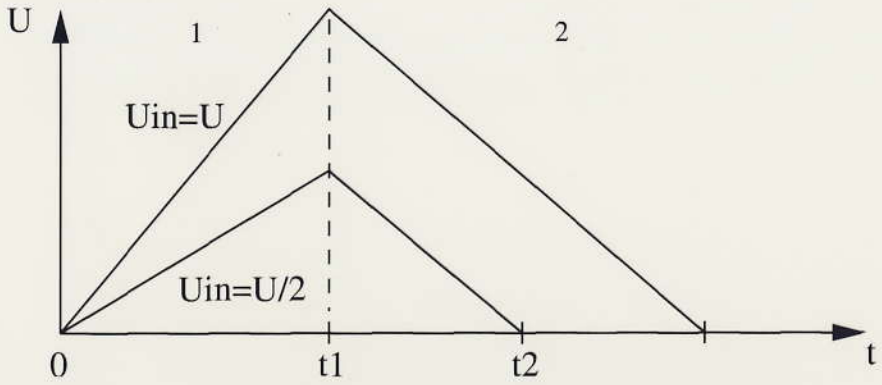
Realisierung

→ Folie

Einsatz: Messtechnik

Dual-Slope Wandler





19-0009; Rev 2; 8/95

EVALUATION KIT MANUAL FOLLOWS DATA SHEET

±18-Bit ADC with Serial Interface

General Description

The MAX132 is a CMOS, 18-bit plus sign, serial-output, analog-to-digital converter (ADC). Multi-slope integration provides high-resolution conversions in less time than standard integrating ADCs, allowing operation up to 100 conversions per second. Low conversion noise provides guaranteed operation with ±512mV full-scale input range (2µV/LSB). A simple 4-wire serial interface connects easily to all common microprocessors, and twos-complement output coding simplifies bipolar measurements. Typical supply current is only 60µA and is reduced to 1µA in sleep mode. Four serially programmed digital outputs can be used to control an external multiplexer or programmable-gain amplifier. The MAX132 comes in 24-pin narrow DIP and wide SO packages, and is available in commercial and extended temperature grades.

High resolution, compact size, and low power make this device ideal for data loggers, weigh scales, data-acquisition systems, and panel meters.

Applications

Remote Data Acquisition

Battery-Powered Instruments

Industrial Process Control

Transducer-Signal Measurement
Pressure, Flow, Temperature, Voltage
Current, Resistance, Weight

Features

- **Low Supply Current:**
  60µA (Normal Operation)
  1µA (Sleep-Mode Operation)
- **±0.006% FSR Accuracy at 16 Conv/sec**
- **Low Noise: 15µV$_{RMS}$**
- **Serial I/O Interface with Programmed Output for Mux and PGA**
- **Performs up to 100 Conv/sec**
- **±2pA Input Current**
- **50Hz/60Hz Rejection**

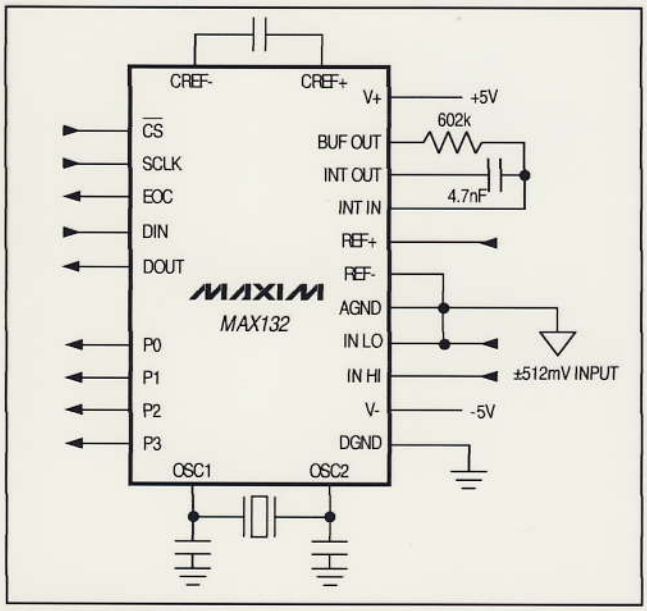
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX132CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX132CWG	0°C to +70°C	24 Wide SO
MAX132C/D	0°C to +70°C	Dice*
MAX132ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX132EWG	-40°C to +85°C	24 Wide SO
MAX132MRG	-55°C to +125°C	24 Narrow CERDIP**

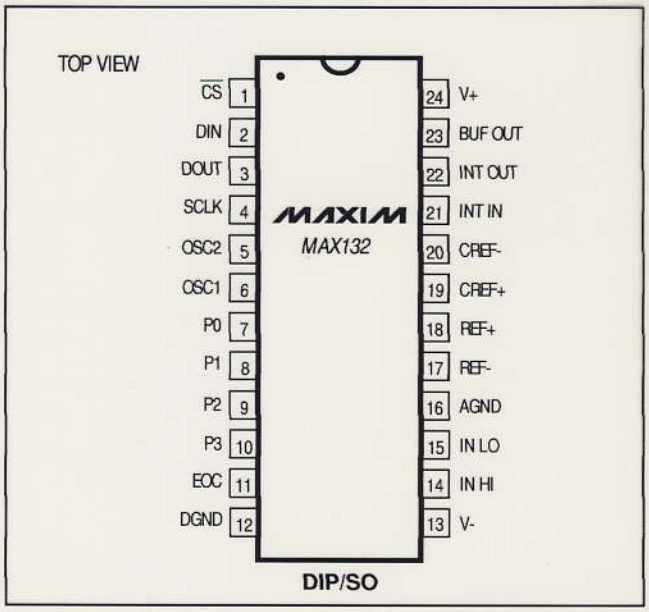
* *Contact factory for dice specifications.*

** *Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



Pin Configuration



±660mV for 60Hz mode operation or between ±390mV and ±550mV for 50Hz mode operation. The pseudo-differential input voltage is applied across pins 14 and 15 (IN HI, IN LO), and can range to within 2V of either supply rail.

The inputs IN HI and IN LO lead directly to CMOS transistor gates, yielding extremely high input impedances that are useful when converting signals from a high input source impedance, such as a sensor. Input currents are only 2pA typical at +25°C. Figure 6 shows an RC filter at the input to optimize noise performance. Fault protection is accomplished by the 100kΩ series resistance. Internal protection diodes, which clamp the analog inputs from V+ to V-, allow the channel input pins to swing from (V- - 0.3V) to (V+ + 0.3V) without damage. However, if the analog input voltage at the pins IN HI or IN LO exceed the supplies, limit the current into the device to less than 1mA, as excessive current will damage the device.

Reference Voltage Selection

The reference voltage sets the analog input voltage range. For the nominal ±512mV full-scale input range, a 545mV reference voltage is used for the 60Hz mode and a 655mV reference voltage is used in the 50Hz mode. The reference voltage can be calculated as follows:

$$\text{60Hz Mode: } V_{REF} = \frac{(545 \text{ counts})\ (512)\ V_{IN(FS)})}{262{,}144}$$

or

$$\text{50Hz Mode: } V_{REF} = \frac{(655 \text{ counts})\ (512)\ V_{IN(FS)})}{262{,}144}$$

The recommended reference voltage range is 500mV to 700mV. The MAX132 is tested with the nominal 545mV reference voltage in 60Hz mode. Use amplifiers or attenuators (resistor dividers) to scale other full-scale input signal ranges to the recommended ±512mV full-scale range.

References outside the recommended range may be used with a degradation of linearity. A reference voltage from 200mV to 500mV will result in a lower signal-to-noise ratio; a reference voltage from 700mV to 2V will increase the rollover error.

The MAX872 2.50V reference, with its 10µA supply current, is ideally suited for the MAX132. Figure 7 shows how 2.50V can be divided to obtain the desired reference voltage. The reference input accepts voltages anywhere within the converter's power-supply range; however, for best performance, neither REF+ nor REF- should come within 2V of the supplies.

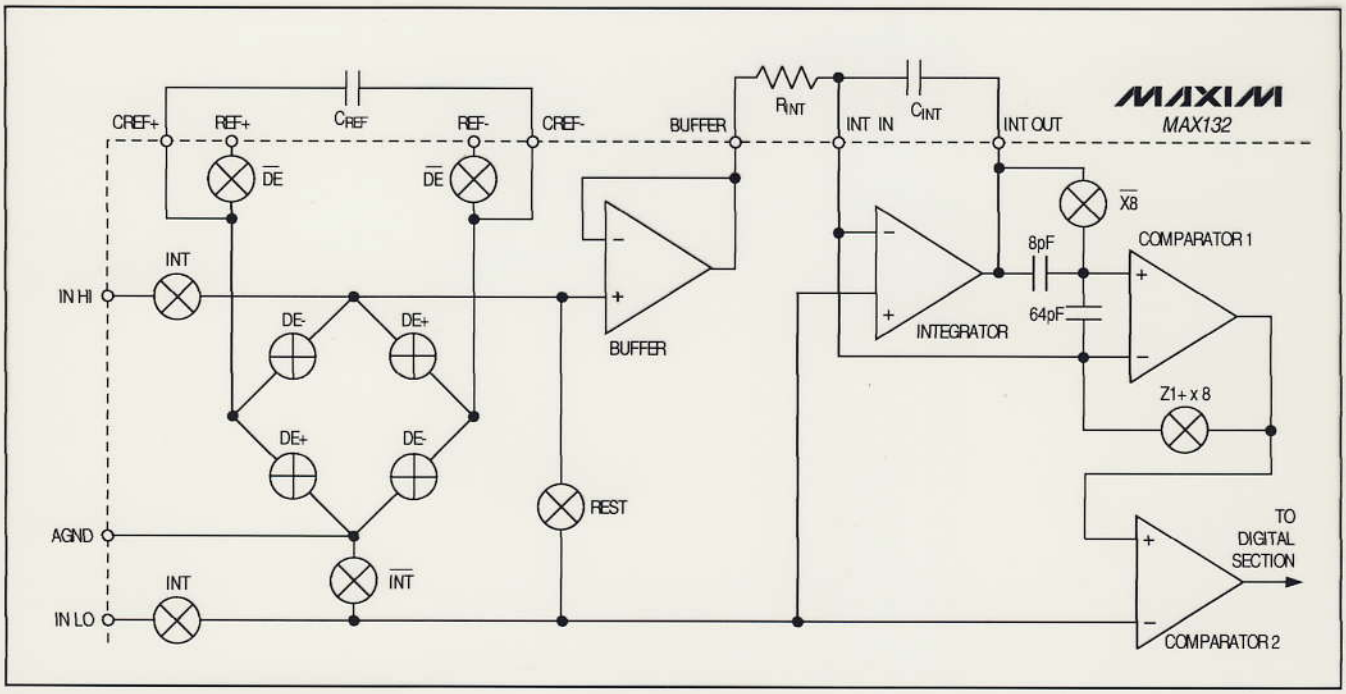
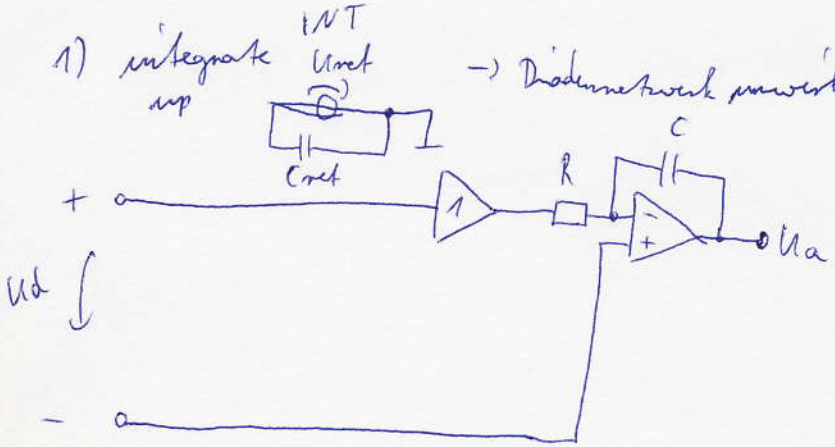


Figure 5. Analog Section Block Diagram

Schalterstellungen

Dual-Slope ADC

1) integrate up

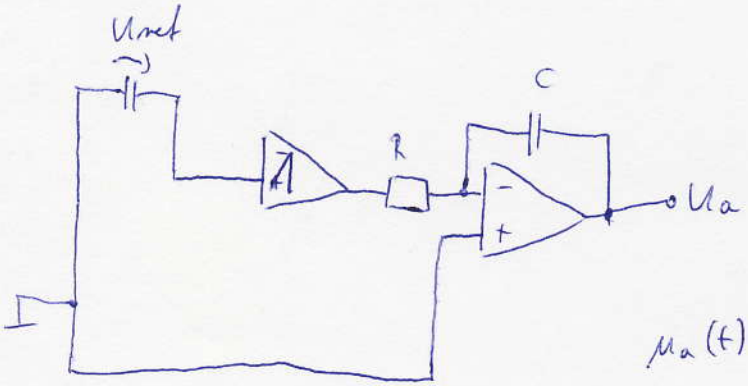


→ Diodennetzwerk unwirksam (DE+, DE-), da deaktiviert

$$u_a(t) = -\int_{t_0}^{t} \frac{u_d(t)}{RC}\,dt + 0$$

$t \leq t_1$

2) integrate down, DE



$$u_a(t) = U(t_1) + \frac{U_{ref}}{RC} \cdot t$$